

# Compal Confidential

## A4WAD MB Schematic Document

### LA-C871P

Rev: 1.0

2015.07.13

DAX

Part Number	Description
DA6001ED010	PCB 1DS LA-C871P REV1 MB 1

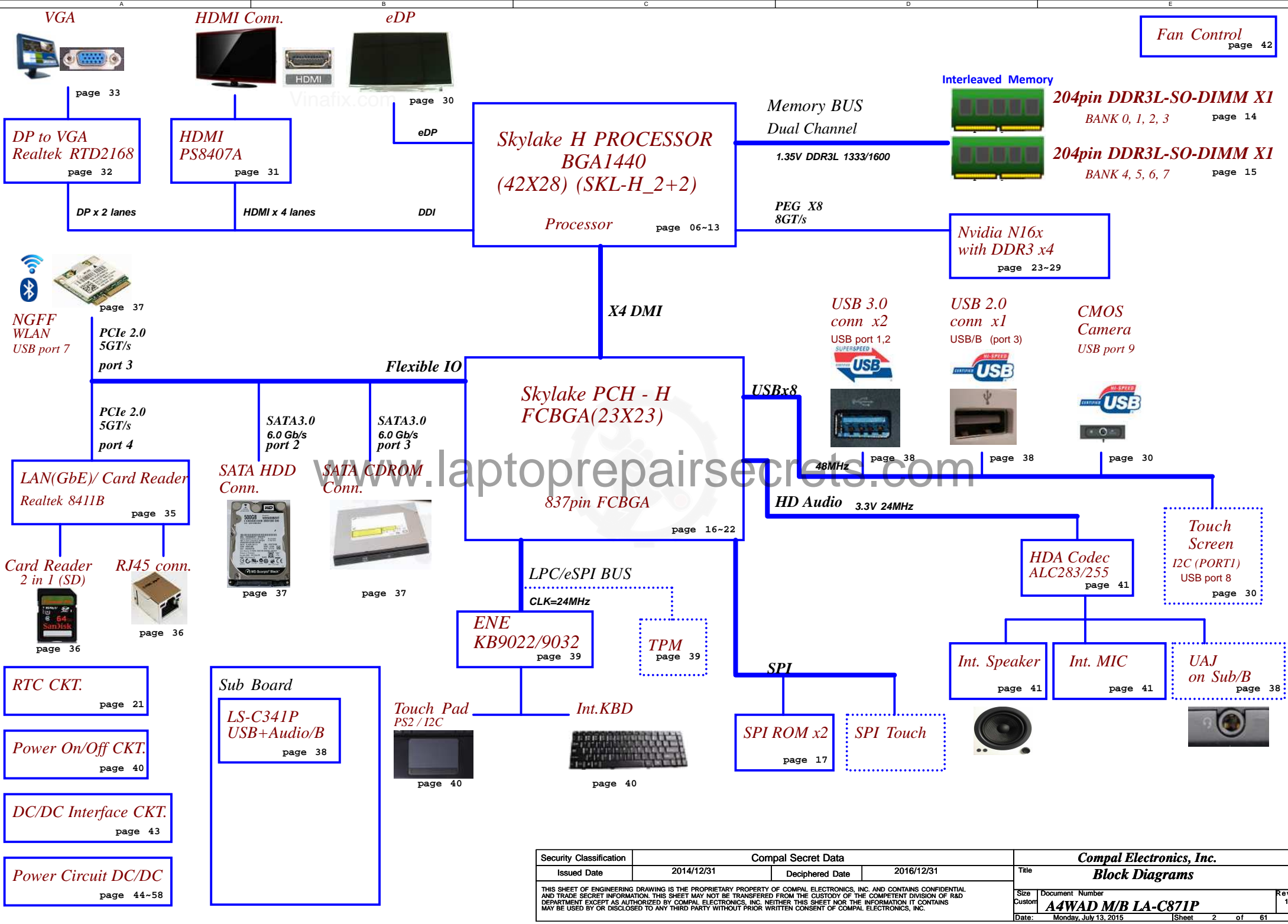
A4WAD\_PCB\_REV10  
PCB@

DAZ

Part Number	Description
DAZ1DS00100	PCB A4WAD LA-C871P LS-C341P

A4WAD\_PCB\_Panelization  
@

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	Cover Sheet	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number	Rev 1.0
				Date: Monday, July 13, 2015	Sheet 1 of 60	



Fan Control  
page 42

VGA  
page 33  
DP to VGA  
Realtek RTD2168  
page 32  
DP x 2 lanes

HDMI Conn.  
HDMI  
PS8407A  
page 31  
HDMI x 4 lanes

eDP  
page 30  
DDI

Skylake H PROCESSOR  
BGA1440  
(42X28) (SKL-H\_2+2)  
Processor  
page 06~13

Memory BUS  
Dual Channel  
1.35V DDR3L 1333/1600  
Interleaved Memory  
204pin DDR3L-SO-DIMM X1  
BANK 0, 1, 2, 3  
page 14  
204pin DDR3L-SO-DIMM X1  
BANK 4, 5, 6, 7  
page 15  
PEG X8  
8GT/s  
Nvidia N16x  
with DDR3 x4  
page 23~29

NGFF  
WLAN  
USB port 7  
page 37  
PCIe 2.0  
5GT/s  
port 3  
PCIe 2.0  
5GT/s  
port 4  
LAN(GbE)/ Card Reader  
Realtek 8411B  
page 35  
Card Reader  
2 in 1 (SD)  
page 36  
RJ45 conn.  
page 36  
SATA HDD  
Conn.  
page 37  
SATA CDROM  
Conn.  
page 37

Skylake PCH - H  
FCBGA(23X23)  
837pin FCBGA  
page 16~22

Flexible IO  
X4 DMI  
USB 3.0  
conn x2  
USB port 1,2  
USB  
48MHz  
page 38  
USB 2.0  
conn x1  
USB/B (port 3)  
USB  
page 38  
CMOS  
Camera  
USB port 9  
page 30  
USB  
page 38  
HD Audio  
3.3V 24MHz  
HDA Codec  
ALC283/255  
page 41  
Touch  
Screen  
I2C (PORT1)  
USB port 8  
page 30  
Int. Speaker  
page 41  
Int. MIC  
page 41  
UAI  
on Sub/B  
page 38  
SPI  
SPI ROM x2  
page 17  
SPI Touch

RTC CKT.  
page 21  
Power On/Off CKT.  
page 40  
DC/DC Interface CKT.  
page 43  
Power Circuit DC/DC  
page 44~58  
Sub Board  
LS-C341P  
USB+Audio/B  
page 38  
Touch Pad  
PS2 / I2C  
page 40  
Int.KBD  
page 40

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title Block Diagrams	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number A4WAD M/B LA-C871P
				Date: Monday, July 13, 2015	Rev 1.0
				Sheet 2	of 61

Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V <sub>BD</sub> min	V <sub>BD</sub> typ	V <sub>BD</sub> max	EC AD3
0	0	0 V	0 V	0.300 V	0x00 - 0x0B
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x0C - 0x1C
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1D - 0x26
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x27 - 0x30
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3B
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3C - 0x46
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x47 - 0x54
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64

BOM Structure Table

BOM Option Table		BOM Option Table	
Item	BOM Structure	Item	BOM Structure
Unpop	@	dGPU	VGA@
Connector	CONN@	N16S-GT	SGT@
EMC requirement	EMC@	N16V-GM	VGM@
EMC requirement depop	@EMC@	Non GPU CG6 funct i on	NGC6@
CODEC(ALC255)	255@	GPU CG6 funct i on	GC6@
CODEC(ALC283)	283@	VRAM BOM Select	X76@
SPI ROM 8M*2	8M_DUAL@	DMIC*1	DMIC@
SPI ROM 8M*1	8M_SINGLE@	For Acer IOAC	IOAC@
UMA only	UMA@	No Acer IOAC	NIOAC@
TPM	TPM@		
CMC	CMC@		
Keyboard backlight	KB@		
LPC MODE for EC	LPC@		
ESPI MODE for EC	ESPI@		
BA Serial	BA@		

I2C Address Table (TBC)

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Touch Panel	reserved		
I2C_1 (+3VS)	TM-P2969-001 (Touch Pad)	0x2C		
	SB8787-1200 (Touch Pad)	0x15		
PCH_SMBCLK (+3VALW)	DIMM1	0xA0		
	DIMM2	0xA4		
	LIS3DHTR(G-sensor)	0x30		
PCH_SML1CLK (+3VALW)	N16S-GT (VGA)	0x9E		
	RTD2168 (CRT)	reserved		
	EC			
EC_SMB_CK1 (+3VLP)	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

43 level BOM table

43 Level	Description	BOM Structure
4319YYBOL01	SMT MB AC871 A4WAD QHR7 1.6G UMA HDMI	QHR7@/1dMIC@/255@/8M_SINGLE@/BA@/EMC@/IOAC@/KB@/LPC@/PCB@/PCH@/TPM@/XDP@/ES@/UMA@
4319YYBOL02	SMT MB AC871 A4WAD QHR7 1.6G GM2G HDMI	QHR7@/1dMIC@/255@/8M_SINGLE@/BA@/EMC@/IOAC@/KB@/LPC@/PCB@/PCH@/TPM@/XDP@/ES@/VGA@/VGM@/NGC6@/X7601@
4319YYBOL03	SMT MB AC871 A4WAD QHPW 2.2G GM2G HDMI	QHPW@/1dMIC@/255@/8M_SINGLE@/BA@/EMC@/IOAC@/KB@/LPC@/PCB@/PCH@/TPM@/XDP@/ES@/VGA@/VGM@/NGC6@/X7601@
4319YYBOL04	SMT MB AC871 A4WAD QHPW 2.2G GT2G HDMI	QHPW@/1dMIC@/255@/8M_SINGLE@/BA@/EMC@/IOAC@/KB@/LPC@/PCB@/PCH@/TPM@/XDP@/ES@/VGA@/SGT@/GC6@/X7603@/

Power State

STATE	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
S0 (Full ON)	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

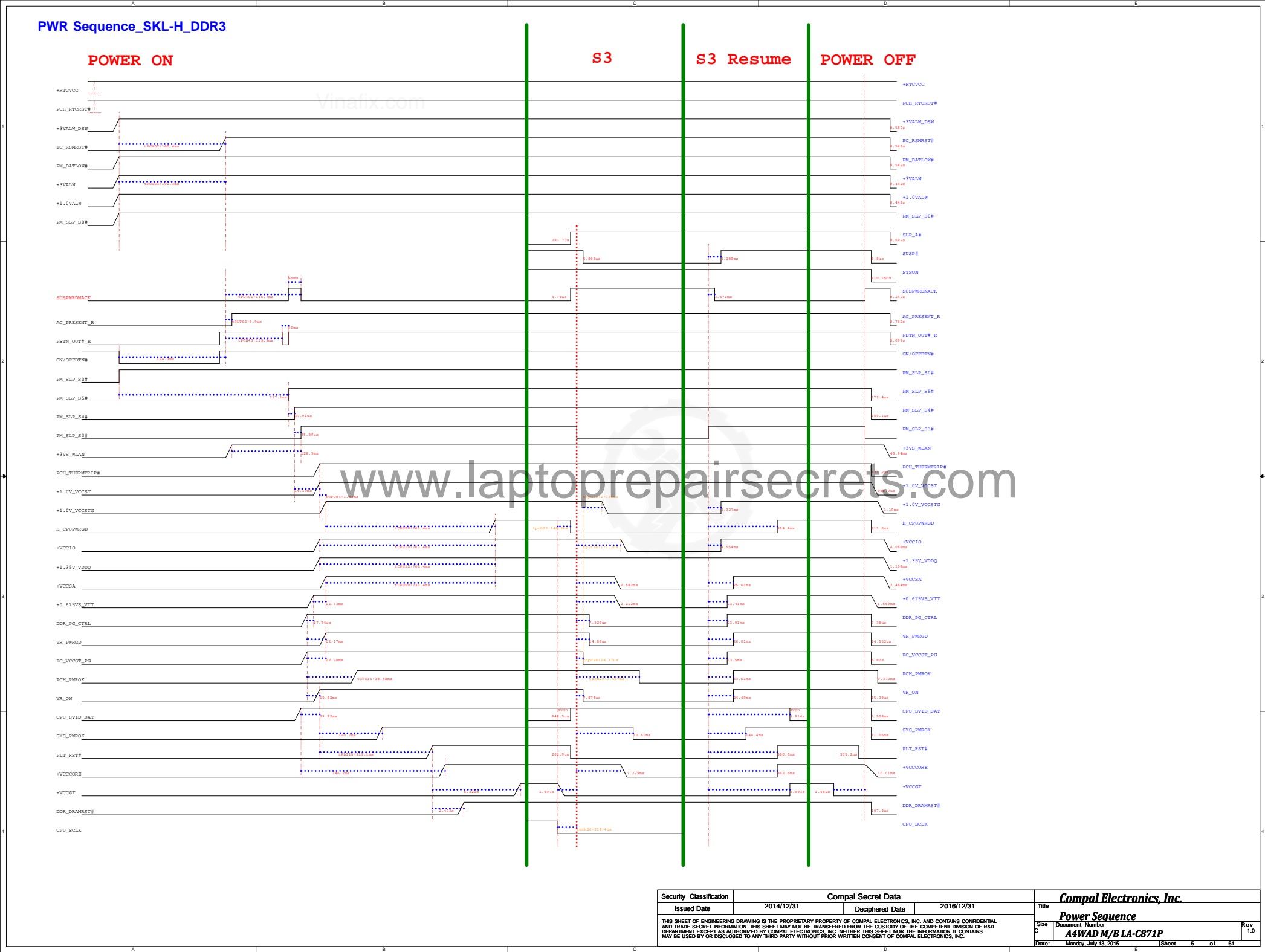
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	0.7
7	0.8

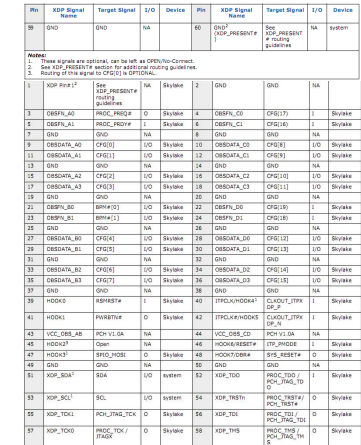
Voltage Rails (TBC)

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
VIN	Adapter power supply	N/A	N/A	N/A	N/A
BATT+	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+3VALW_PCH	+3VALW power for PCH power rails	ON	ON	ON	ON*
+3VALW_SPI	+3VALW_PRIM supply for the SPI IO	ON	ON	ON	ON
+1.0VALW	+1.0V Always power rail	ON	ON	ON	ON
+1.35V_VDDQ	DDRIII/L-RS +1.35V power rail	ON	ON	OFF	OFF
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.675VS_VTT	DDR +0.675VS power rail for DDR terminator	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+3VSDGPU_AON	+3VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+3VSDGPU_MAIN	+3VS power rail for GPU GC62.0	ON	OFF	OFF	OFF
+VGA_CORE	Core voltage for VGA	ON	OFF	OFF	OFF
+1.8VSDGPU	+1.8VS power rail for GPU	ON	OFF	OFF	OFF
+1.5VSDGPU	+1.5VS power rail for GPU	ON	OFF	OFF	OFF
+1.05VSDGPU	+1.05VS power rail for GPU	ON	OFF	OFF	OFF
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.					

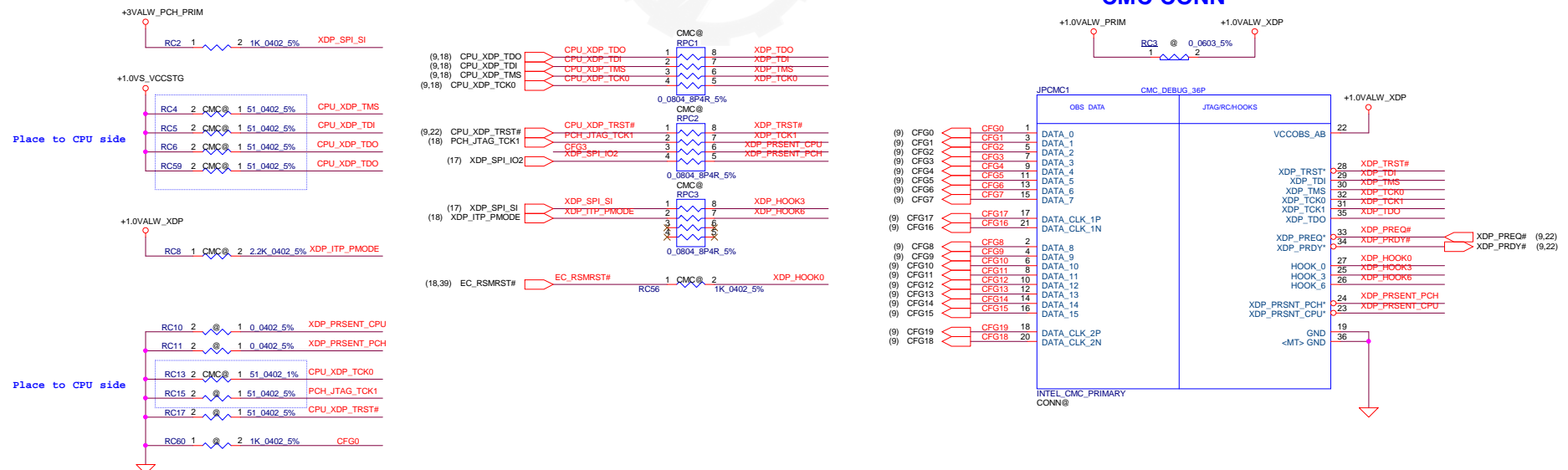


PWR Sequence\_SKL-H\_DDR3





**CMC CONN**

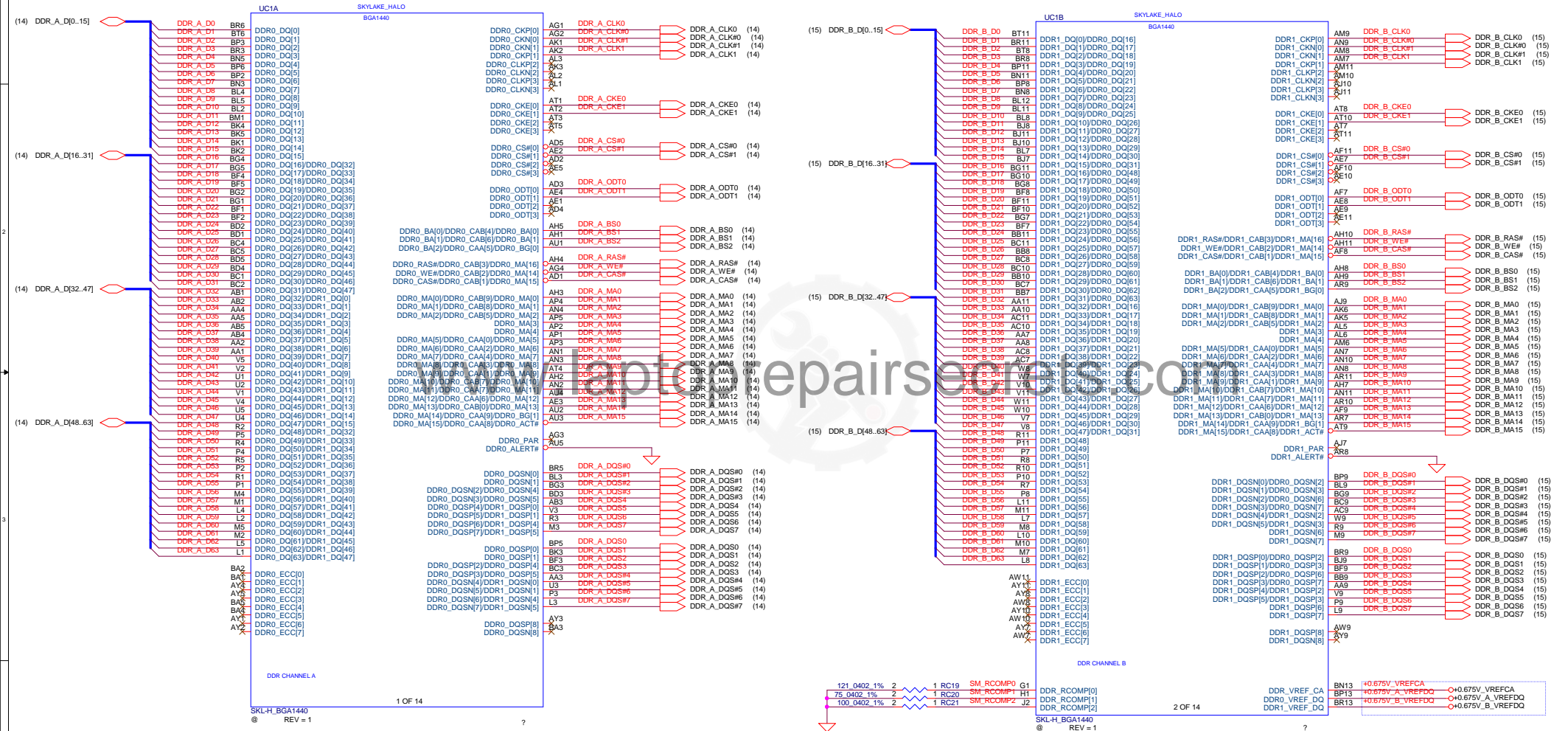


Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>SKL-H(1/9)DDI.EDP</b>	
Issued Date	2014/12/31	Deciphered Date	2016/12/31		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title <b>SKL-H(1/9)DDI.EDP</b>	Rev <b>1.0</b>
				Size <b>A4WAD M/B LA-C871P</b>	
Date:		Monday, July 13, 2015		Sheet 6 of 61	

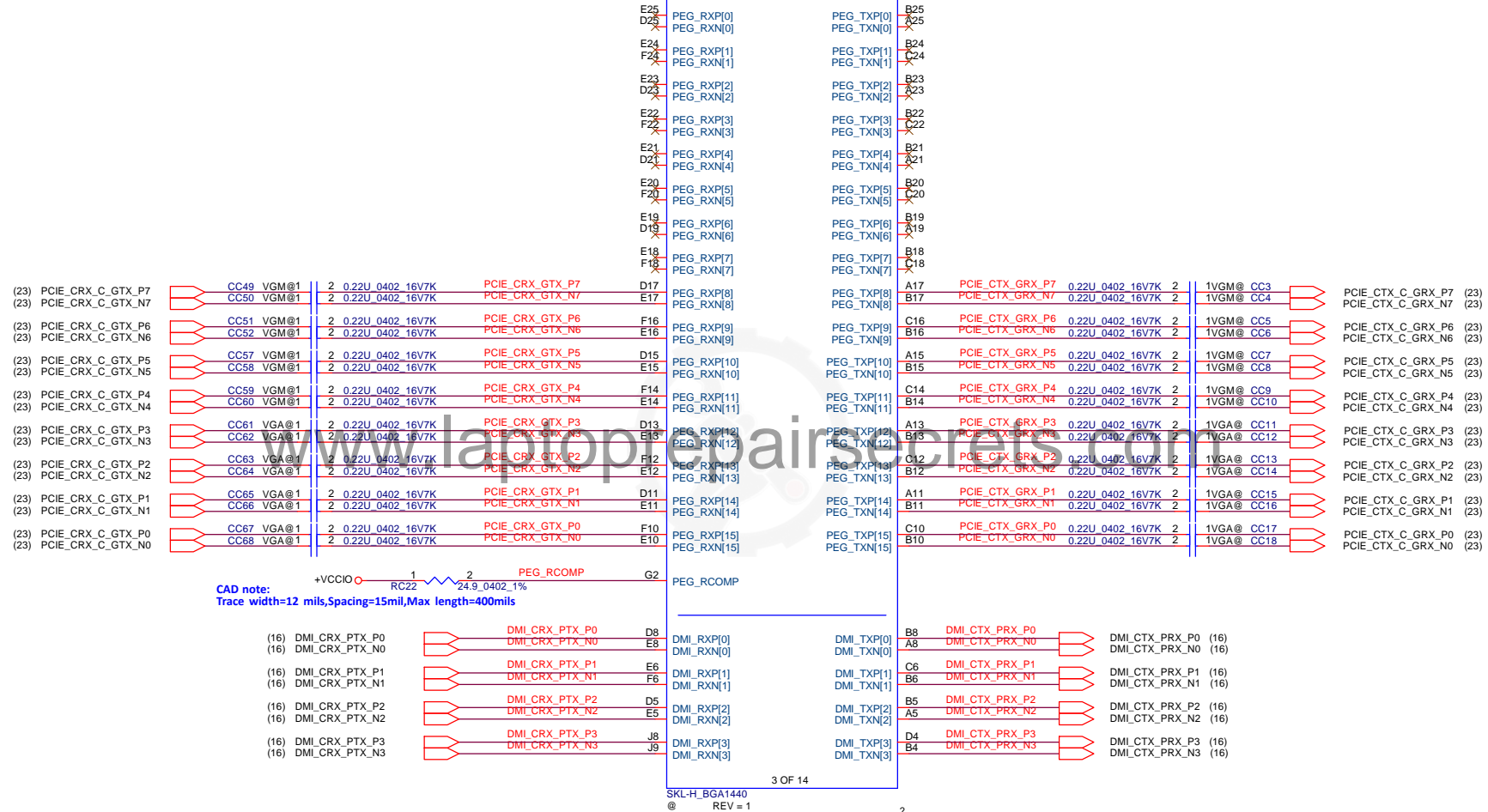


# Interleaved Memory

Vinafix.com



UC1C	SKYLAKE_HALO
	BGA1440



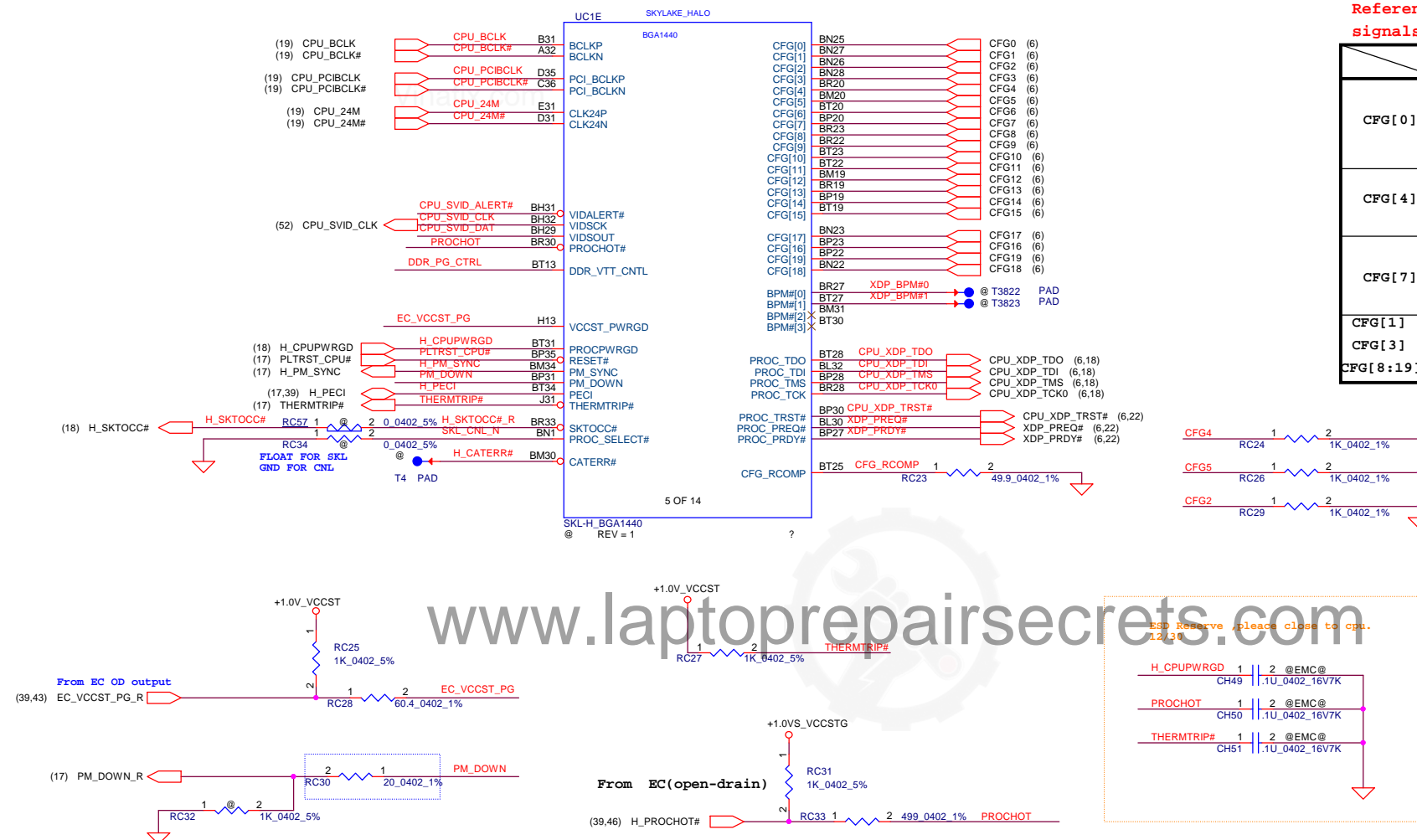
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>SKL-H(3/9) PEG,DMI</b>	
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number <b>A4WAD M/B LA-C871P</b>
				Date: Monday, July 13, 2015	Sheet 8 of 61 Rev 1.0



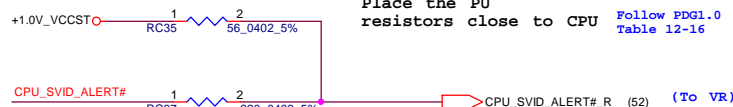
Reference SKL EDS 0.85 Table 6-8CFG  
signals internal PH default value = 1

	Description
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted - 1 = (Default) Normal Operation; - 0 = Stall.
CFG[4]	Enable eDP - 1 = Disabled. - 0 = Enabled.
CFG[7]	PEG Training: - 1 = (default) PEG Train immediately following RESET# de assertion. - 0 = PEG Wait for BIOS for training
CFG[1] CFG[3] CFG[8:19]	Reserved configuration lane.

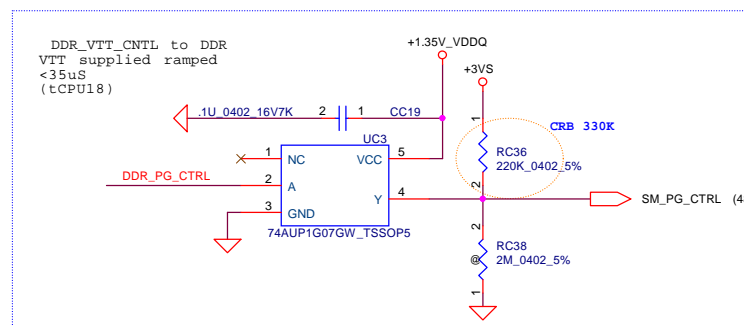
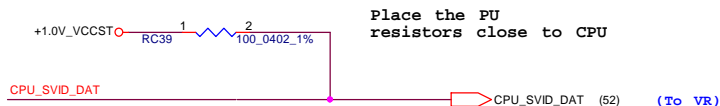
PCIe pore assign	Config. Signals		
	CFG[6]	CFG[5]	CFG[2]
1 x 16	1	1	1
1 x 16 reverse	1	1	0
2 x 8	1	0	1
2 x 8 * reverse	1	0	0
1 x 8 + 2 x 4	0	0	1
1x8+2x4 reverse	0	0	0



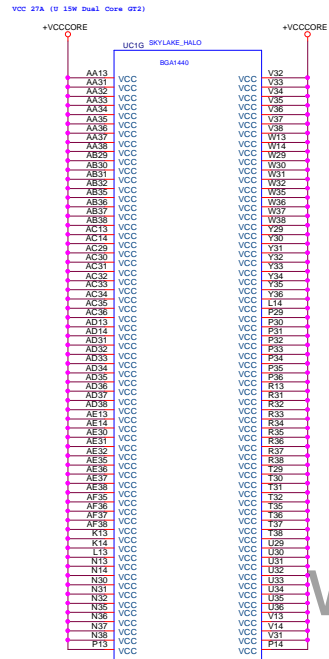
### SVID ALERT



### SVID DATA

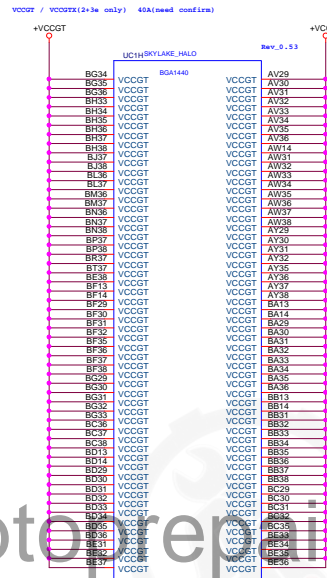


Security Classification			Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	SKL-H(4/9)CLK,GPIO	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Custom	Document Number	Rev 1.0
				Date:	A4WAD M/B LA-C871P	Monday, July 13, 2015
				Sheet	9	of 61

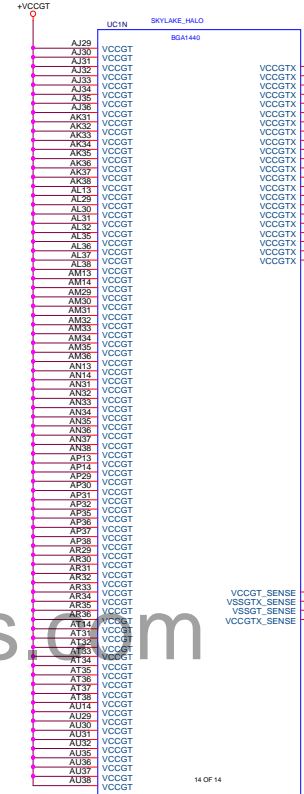


Trace Length < 25 mils

AC37  
AC38  
VCCSENSE (S2)  
VSSSENSE (S2)  
PE/PL on pwr side  
10/07 Dan



Trace Length < 25 mils



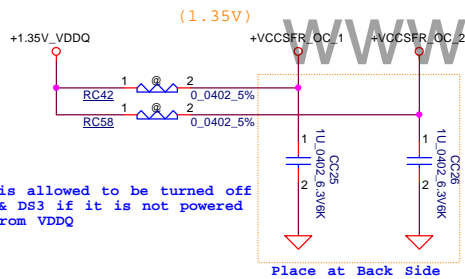
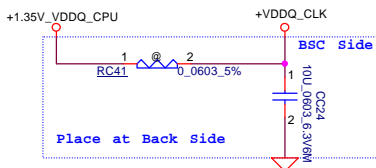
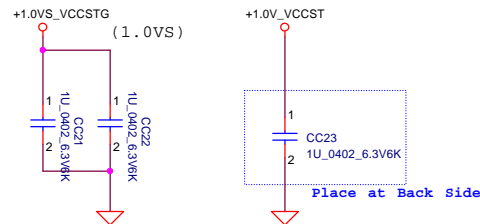
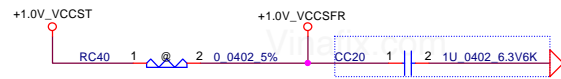
RDS:Rail is unconnected for Processors without QF3/4.

VCCGT\_SENSE  
VSSGT\_SENSE  
VSSGT\_SENSE (S2)  
VSSGT\_SENSE (S2)

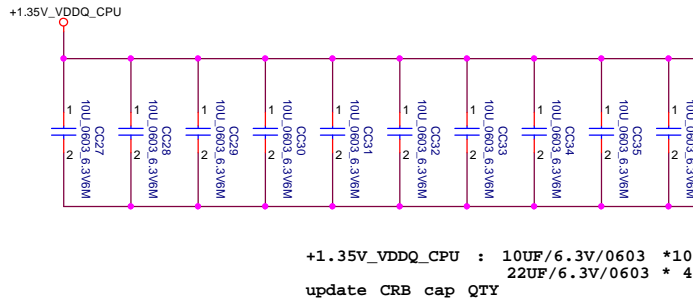
Trace Length < 25 mils

Change to 14/14  
Loss 13 of 14

Security Classification		Compal Secret Data		Compal Electronics, Inc.			
Issued Date		2014/12/31		Deciphered Date		2016/12/31	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title		SKL-H(5/9)Power.SVID	
				Size		Document Number	
				Custom		A4WAD M/B LA-C871P	
				Date		Monday, July 13, 2015	
				Sheet		10 of 61	



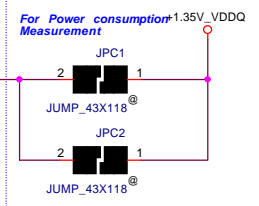
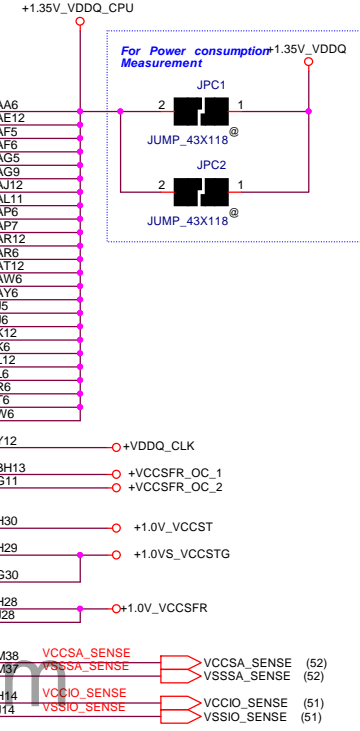
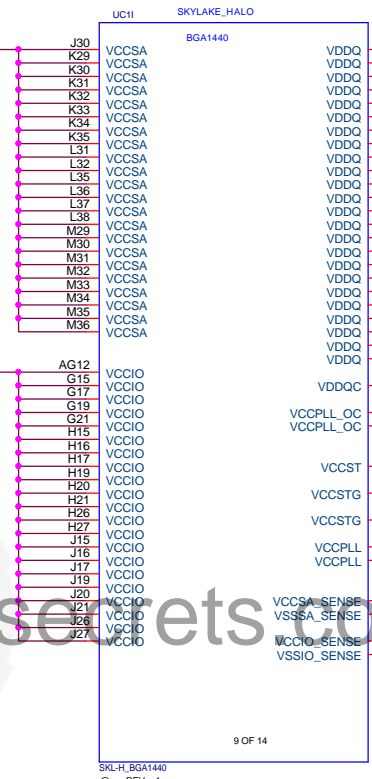
NOTE:  
VCCPLL\_OC is allowed to be turned off during S3 & DS3 if it is not powered directly from VDDQ



+1.35V\_VDDQ\_CPU : 10UF/6.3V/0603 \*10  
22UF/6.3V/0603 \* 4  
update CRB cap QTY

RVF11 47u\*1,10u\*7,1u\*3  
CAP place on PWR side.  
+VCCSA

RVF11  
PWR NEED PROVIDE +VCCIO  
0.95V FOR VCCIO

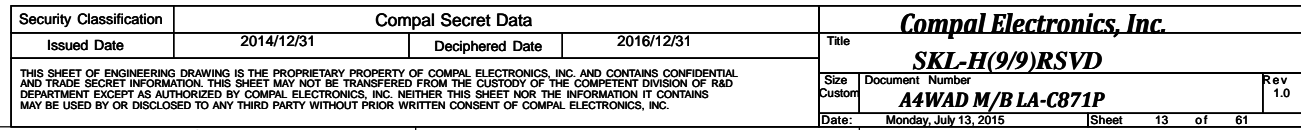


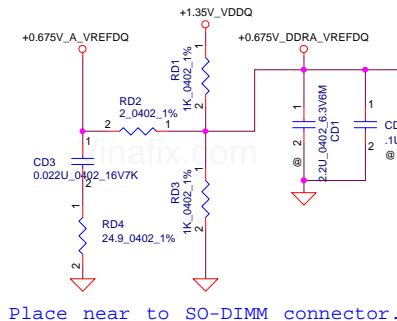
Follow ORB 3/20

CPU\_CORE/VCCGT/VCCSA decoupling capacitor place to PWR side

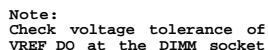
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>			
Issued Date		2014/12/31	Deciphered Date	2016/12/31	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					<b>SKL-H(6/9)POWER</b>		
					Size	Document Number	Rev
					Custm	<b>A4WAD M/B LA-C871P</b>	1.0
					Date:	Monday, July 13, 2015	Sheet 11 of 61







Place near to SO-DIMM connector.



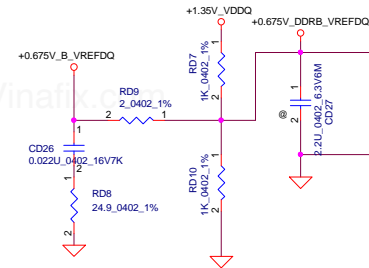
Layout Note:  
Place near JDIMM1.199



## Interleaved Memory

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>			
Issued Date		2014/12/31		Deciphered Date		2016/12/31	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Title			
				<b>DDR3L DIMMA</b>			
				Size	Document	Number	Rev
		Custm					1.0
		<b>A4WAD M/B LA-C871P</b>					
		Date:	Monday, July 13, 2015		Sheet	14	of 61

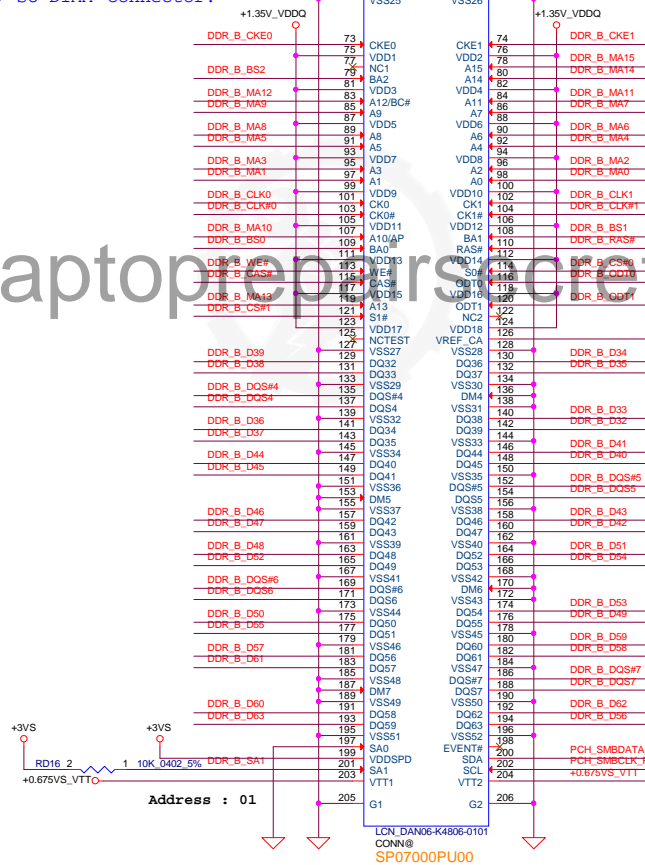




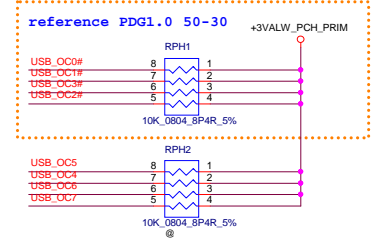
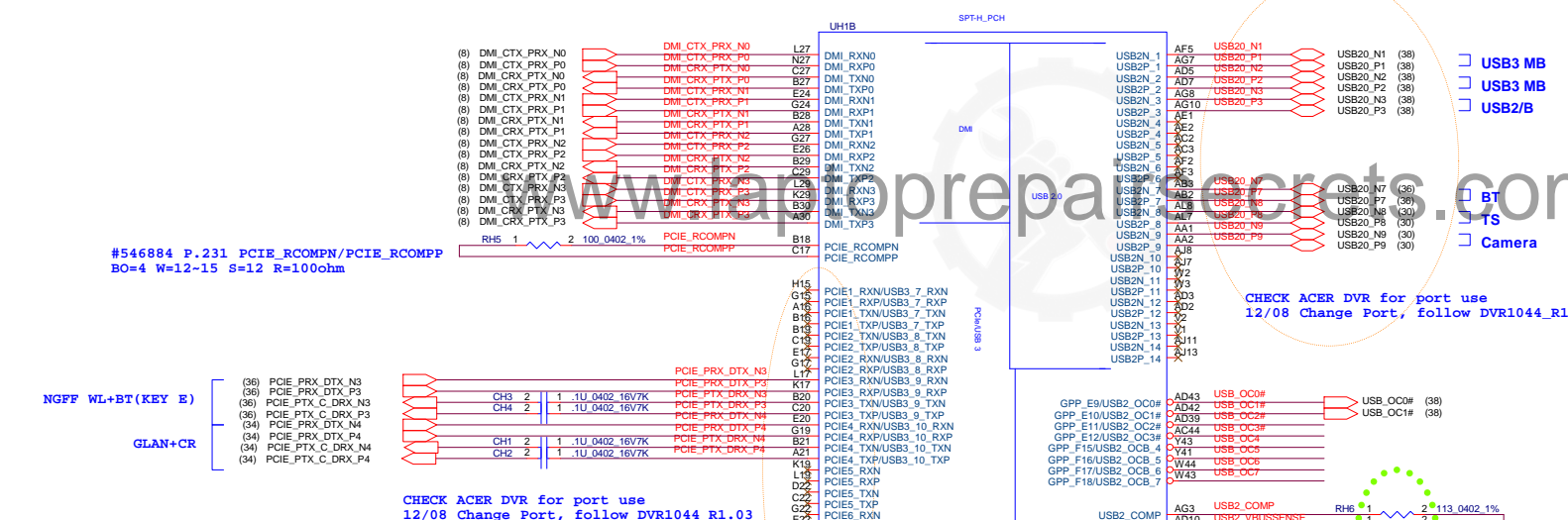
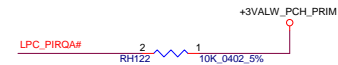
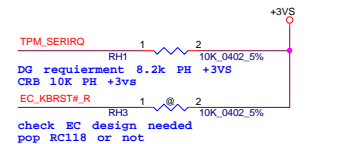
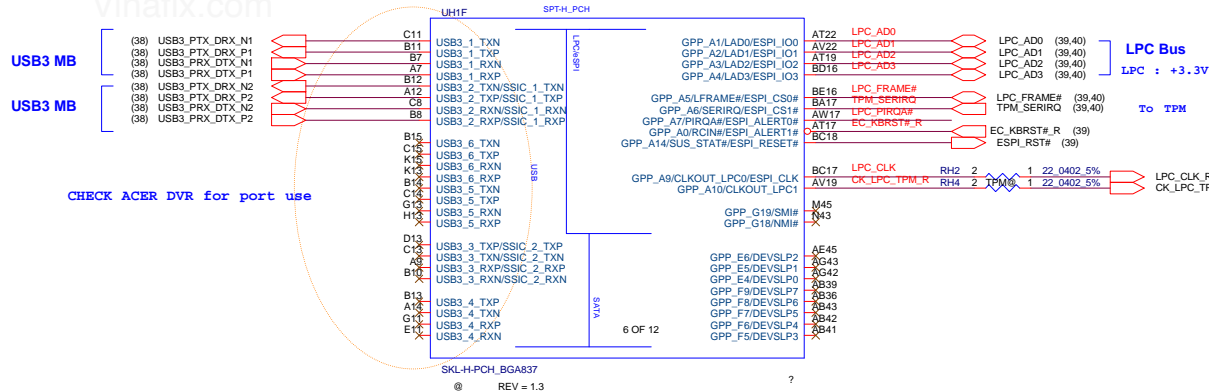
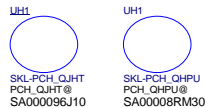
Place near to SO-DIMM connector.



Layout Note:  
Place near JDIMM2.199



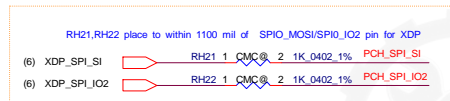
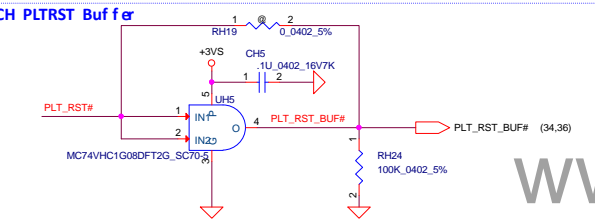
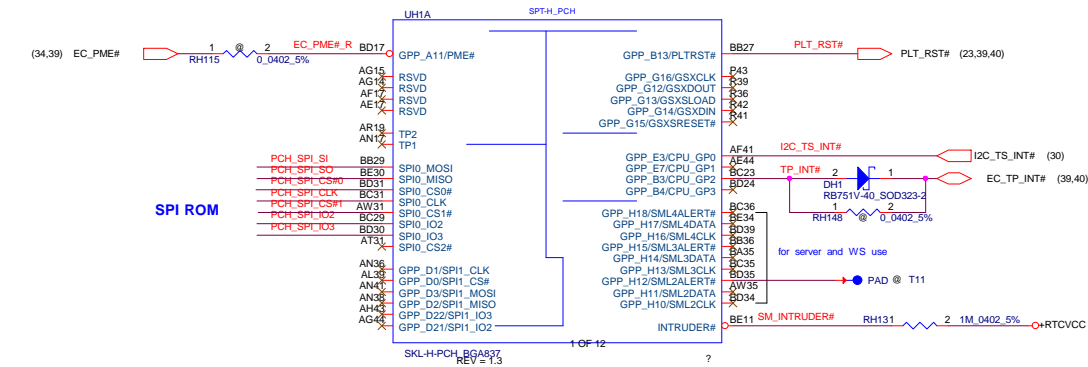
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>DDR3L_DIMMB</b>	
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Custom Document Number <b>A4WAD M/B LA-C871P</b>	1.0
Date:		Monday, July 13, 2015		Sheet	15 of 61



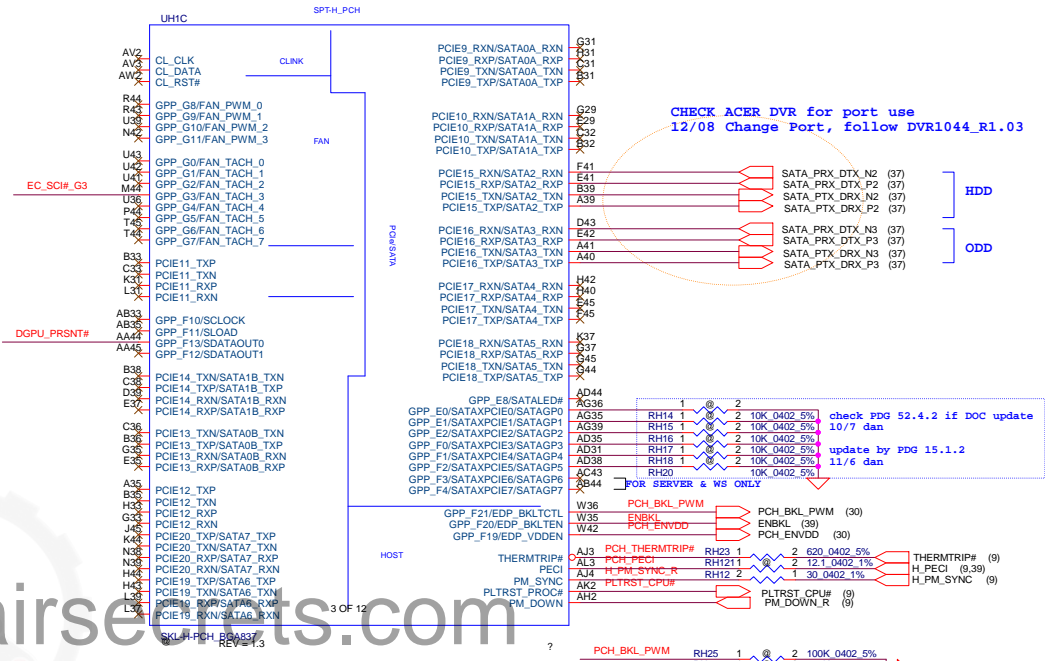
3.4 Intel SKYLAKE two chip.	
Lane1	USB3 Port1
Lane2	USB3 Port2
Lane3	USB3 Port3
Lane4	USB3 Port4
Lane5	USB3 Port5
Lane6	USB3 Port6
Lane7	USB3 Port7
Lane8	USB3 Port8
Lane9	USB3 Port9
Lane10	USB3 Port10
Lane11	USB3 Port11
Lane12	USB3 Port12
Lane13	USB3 Port13
Lane14	USB3 Port14
Lane15	USB3 Port15
Lane16	USB3 Port16
Lane17	USB3 Port17
Lane18	USB3 Port18
Lane19	USB3 Port19
Lane20	USB3 Port20
Lane21	USB3 Port21
Lane22	USB3 Port22
Lane23	USB3 Port23
Lane24	USB3 Port24
Lane25	USB3 Port25
Lane26	USB3 Port26
Lane27	USB3 Port27
Lane28	USB3 Port28
Lane29	USB3 Port29
Lane30	USB3 Port30
Lane31	USB3 Port31
Lane32	USB3 Port32
Lane33	USB3 Port33
Lane34	USB3 Port34
Lane35	USB3 Port35
Lane36	USB3 Port36
Lane37	USB3 Port37
Lane38	USB3 Port38
Lane39	USB3 Port39
Lane40	USB3 Port40
Lane41	USB3 Port41
Lane42	USB3 Port42
Lane43	USB3 Port43
Lane44	USB3 Port44
Lane45	USB3 Port45
Lane46	USB3 Port46
Lane47	USB3 Port47
Lane48	USB3 Port48
Lane49	USB3 Port49
Lane50	USB3 Port50

Acet 2015	
USB3 (U0)	USB3 (U0)
USB3 (U1)	USB3 (U1)
USB3 (U2)	USB3 (U2)
USB3 (U3)	USB3 (U3)
USB3 (U4)	USB3 (U4)
USB3 (U5)	USB3 (U5)
USB3 (U6)	USB3 (U6)
USB3 (U7)	USB3 (U7)
USB3 (U8)	USB3 (U8)
USB3 (U9)	USB3 (U9)
USB3 (U10)	USB3 (U10)
USB3 (U11)	USB3 (U11)
USB3 (U12)	USB3 (U12)
USB3 (U13)	USB3 (U13)
USB3 (U14)	USB3 (U14)
USB3 (U15)	USB3 (U15)
USB3 (U16)	USB3 (U16)
USB3 (U17)	USB3 (U17)
USB3 (U18)	USB3 (U18)
USB3 (U19)	USB3 (U19)
USB3 (U20)	USB3 (U20)
USB3 (U21)	USB3 (U21)
USB3 (U22)	USB3 (U22)
USB3 (U23)	USB3 (U23)
USB3 (U24)	USB3 (U24)
USB3 (U25)	USB3 (U25)
USB3 (U26)	USB3 (U26)
USB3 (U27)	USB3 (U27)
USB3 (U28)	USB3 (U28)
USB3 (U29)	USB3 (U29)
USB3 (U30)	USB3 (U30)
USB3 (U31)	USB3 (U31)
USB3 (U32)	USB3 (U32)
USB3 (U33)	USB3 (U33)
USB3 (U34)	USB3 (U34)
USB3 (U35)	USB3 (U35)
USB3 (U36)	USB3 (U36)
USB3 (U37)	USB3 (U37)
USB3 (U38)	USB3 (U38)
USB3 (U39)	USB3 (U39)
USB3 (U40)	USB3 (U40)
USB3 (U41)	USB3 (U41)
USB3 (U42)	USB3 (U42)
USB3 (U43)	USB3 (U43)
USB3 (U44)	USB3 (U44)
USB3 (U45)	USB3 (U45)
USB3 (U46)	USB3 (U46)
USB3 (U47)	USB3 (U47)
USB3 (U48)	USB3 (U48)
USB3 (U49)	USB3 (U49)
USB3 (U50)	USB3 (U50)

Rebin_SLS (ARMV8)	
USB3 (U0)	USB3 (U0)
USB3 (U1)	USB3 (U1)
USB3 (U2)	USB3 (U2)
USB3 (U3)	USB3 (U3)
USB3 (U4)	USB3 (U4)
USB3 (U5)	USB3 (U5)
USB3 (U6)	USB3 (U6)
USB3 (U7)	USB3 (U7)
USB3 (U8)	USB3 (U8)
USB3 (U9)	USB3 (U9)
USB3 (U10)	USB3 (U10)
USB3 (U11)	USB3 (U11)
USB3 (U12)	USB3 (U12)
USB3 (U13)	USB3 (U13)
USB3 (U14)	USB3 (U14)
USB3 (U15)	USB3 (U15)
USB3 (U16)	USB3 (U16)
USB3 (U17)	USB3 (U17)
USB3 (U18)	USB3 (U18)
USB3 (U19)	USB3 (U19)
USB3 (U20)	USB3 (U20)
USB3 (U21)	USB3 (U21)
USB3 (U22)	USB3 (U22)
USB3 (U23)	USB3 (U23)
USB3 (U24)	USB3 (U24)
USB3 (U25)	USB3 (U25)
USB3 (U26)	USB3 (U26)
USB3 (U27)	USB3 (U27)
USB3 (U28)	USB3 (U28)
USB3 (U29)	USB3 (U29)
USB3 (U30)	USB3 (U30)
USB3 (U31)	USB3 (U31)
USB3 (U32)	USB3 (U32)
USB3 (U33)	USB3 (U33)
USB3 (U34)	USB3 (U34)
USB3 (U35)	USB3 (U35)
USB3 (U36)	USB3 (U36)
USB3 (U37)	USB3 (U37)
USB3 (U38)	USB3 (U38)
USB3 (U39)	USB3 (U39)
USB3 (U40)	USB3 (U40)
USB3 (U41)	USB3 (U41)
USB3 (U42)	USB3 (U42)
USB3 (U43)	USB3 (U43)
USB3 (U44)	USB3 (U44)
USB3 (U45)	USB3 (U45)
USB3 (U46)	USB3 (U46)
USB3 (U47)	USB3 (U47)
USB3 (U48)	USB3 (U48)
USB3 (U49)	USB3 (U49)
USB3 (U50)	USB3 (U50)

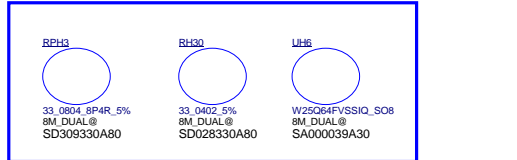
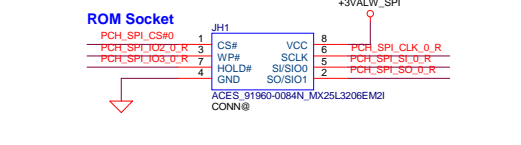
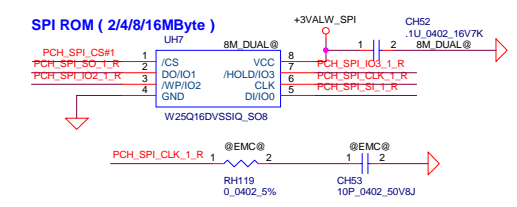
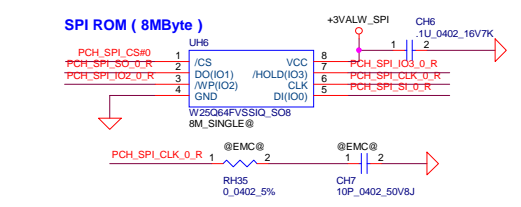
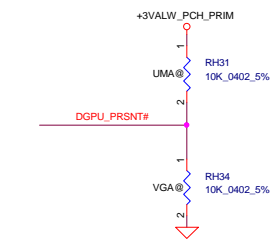
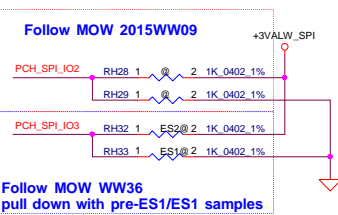
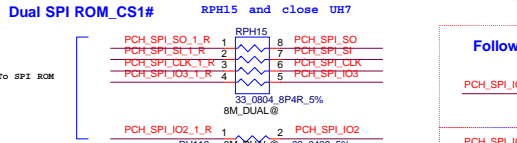
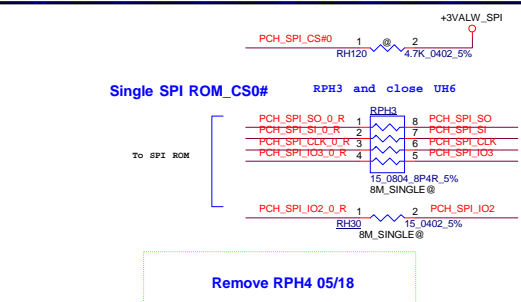


www.laptoprepairsecrets.com



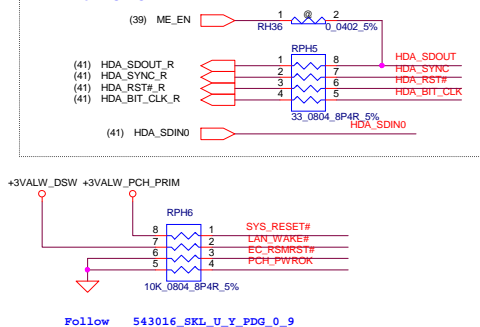
### Functional Strap Definitions

- SPI0\_MOSI**  
int. PH  
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
- SPI0\_MISO**  
int. PH  
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
- SPI0\_IQ2**  
int. PH  
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
- SPI0\_IQ3**  
int. PH  
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

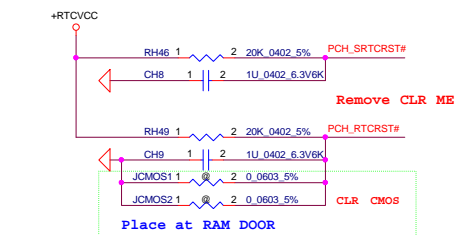
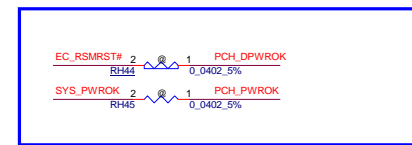
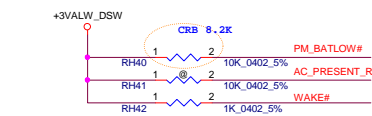


	GPP_F13
DIS,Optimus	0
UMA	1

## HDA for AUDIO



Follow [543016\\_SKL\\_U\\_Y\\_PDG\\_0\\_9](#)



## Functional Strap Definitions

**SMBALERT# / GPP\_C2**  
**int. PD**  
**0 = Disable Intel ME (TLS) (Default)**  
**1 = Enable Intel ME (TLS)**

**SML0ALERT# / GPP\_C5**  
**int. PD**  
**0 = LPC Is selected for EC. (Default)**  
**1 = eSPI Is selected for EC.**

SML1ALERT# / PCHHOT# / GPP\_B23  
int. PD

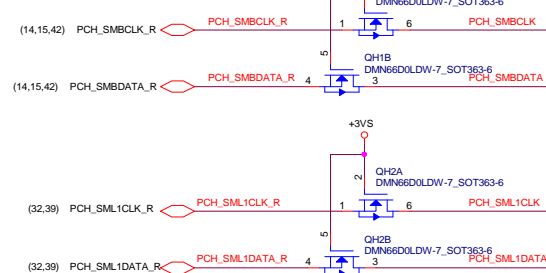
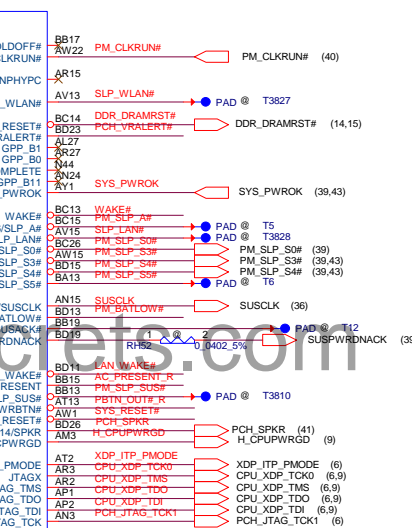
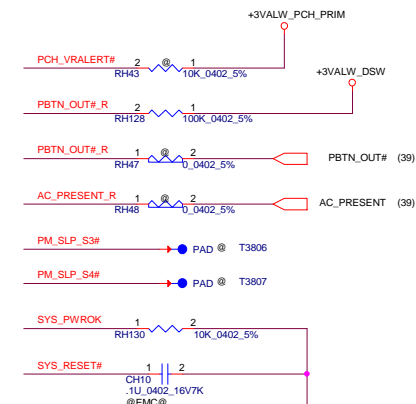
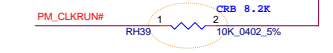
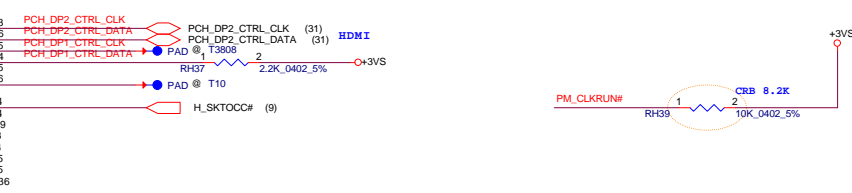
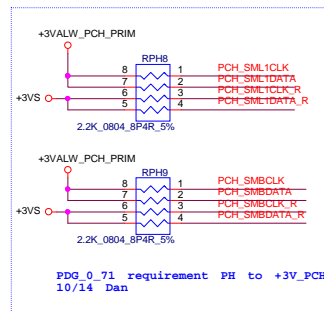
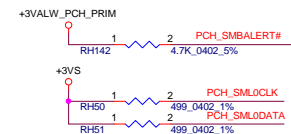
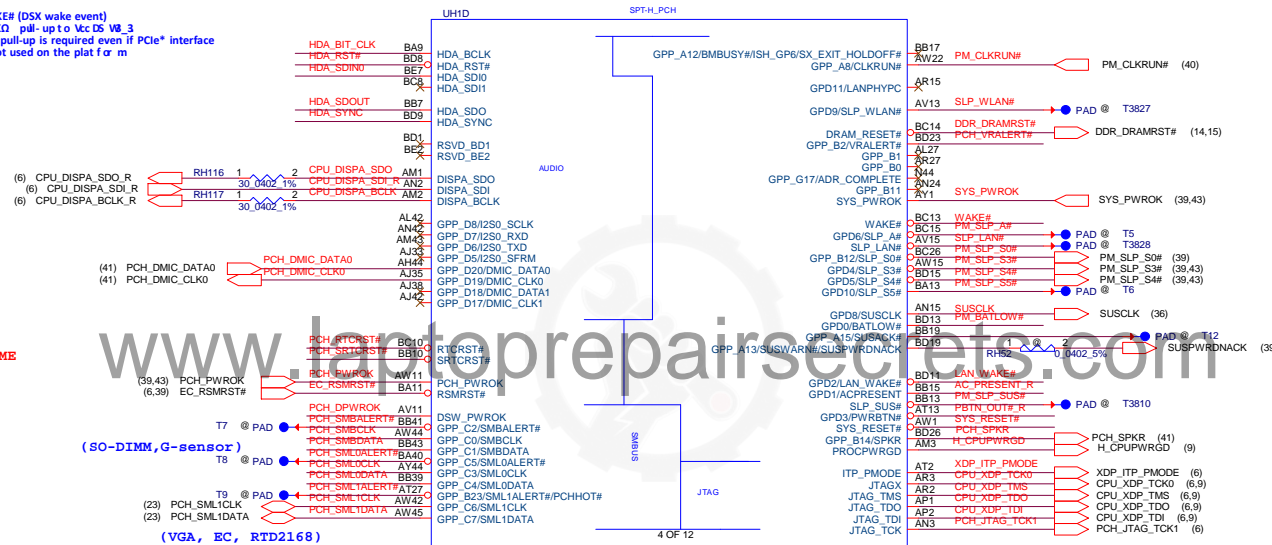
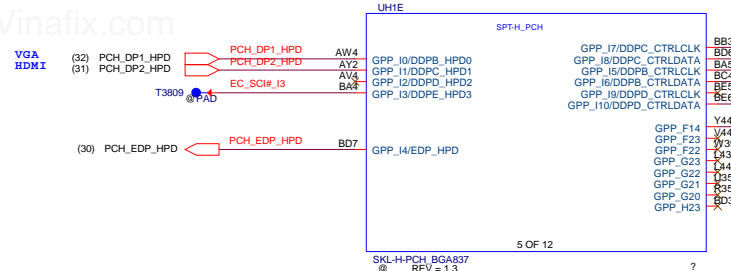
SPKR / GPP\_B14  
int. PD  
0 = Disable " Top Swap" mode (Def alt)  
1 = Enable " Top Swap" mode.

**HDA\_SDO**  
int. PD  
0 = Enable security measures defined in the Flash Descriptor. (Default)  
1 = Disable Flash Descriptor Security (override).

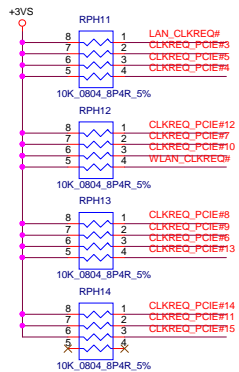
**DDPB\_CTRLDATA / GPP\_I6**  
int. PD  
0 = Port B is not detected.  
1 = Port B is detected. (Default)

DDPC\_CTRLDATA / GPP\_I8  
int. PD  
0 = Port C is not detected.  
1 = Port C is detected. (Default)

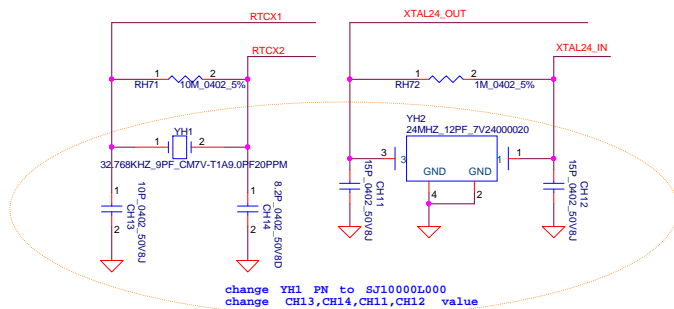
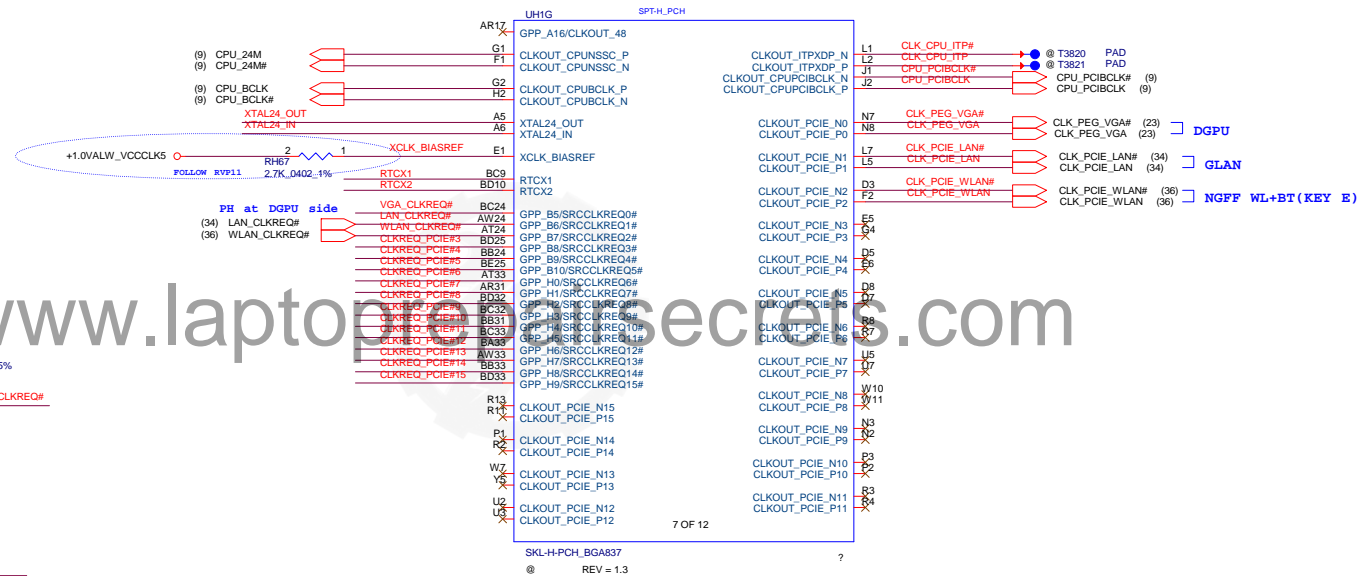
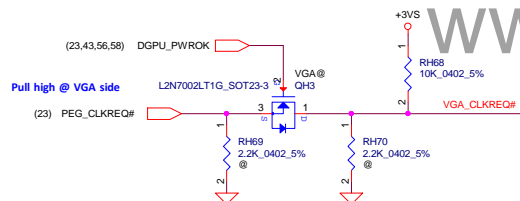
DDPD\_CTRLDATA / GPP\_10  
int. PD  
0 = Port D is not detected. (Default)  
1 = Port D is detected.



Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>PCH(37)GPIO, SMBUS</b>	
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Custom	1.0
				Document Number	
				<b>A4AWD M/B LA-C871P</b>	
				Date: Monday, July 13, 2015	Sheet 18 of 61



Follow PDG 0.71 Table 52-17  
10/13 Dan  
CHECK NEEDED IF UNUSE?



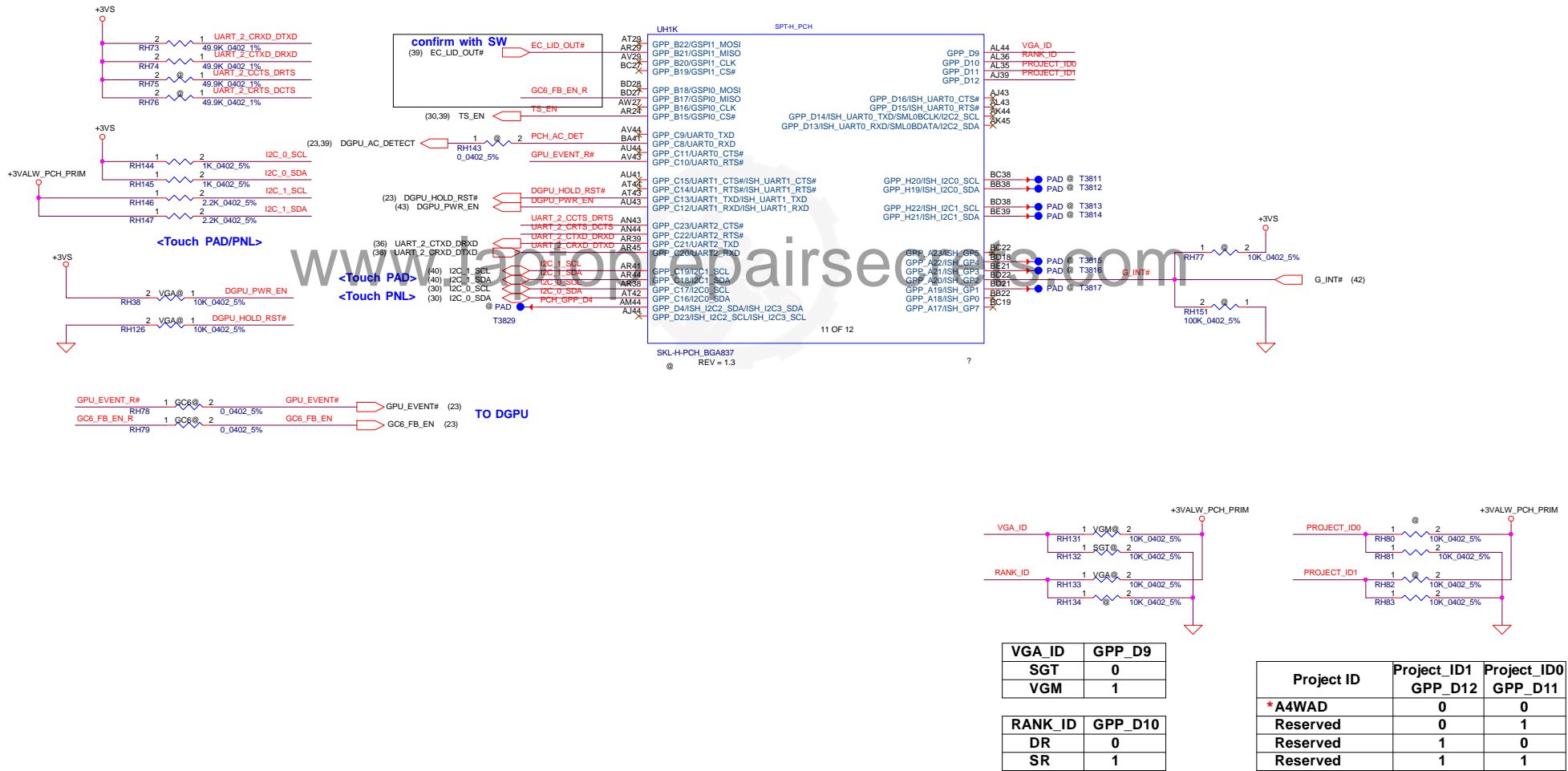
change YH1 PN to SJ10000L000  
change CH13, CH14, CH11, CH12 value



Functional Strap Definitions

GSP11\_MOSI / GPP\_B22  
int. PD  
Boot BIOS Destination  
0 = SPI (Default)  
1 = LPC

GSP10\_MOSI / GPP\_B18  
int. PD  
0 = Disable " No Reboot " mode (Default)  
1 = Enable " No Reboot " mode (PCI will disable the TCO  
Timer system reboot feature).

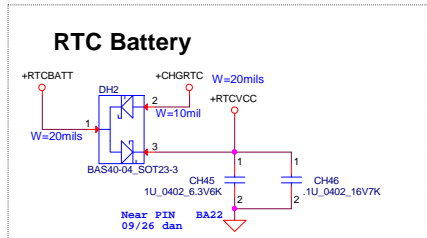
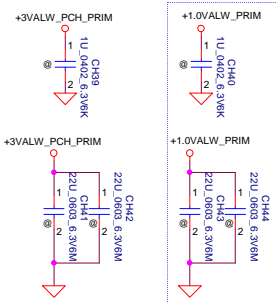
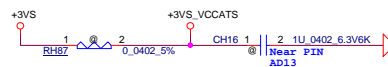
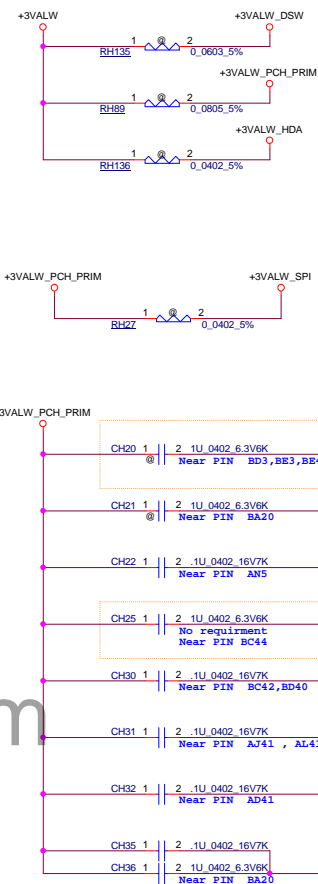
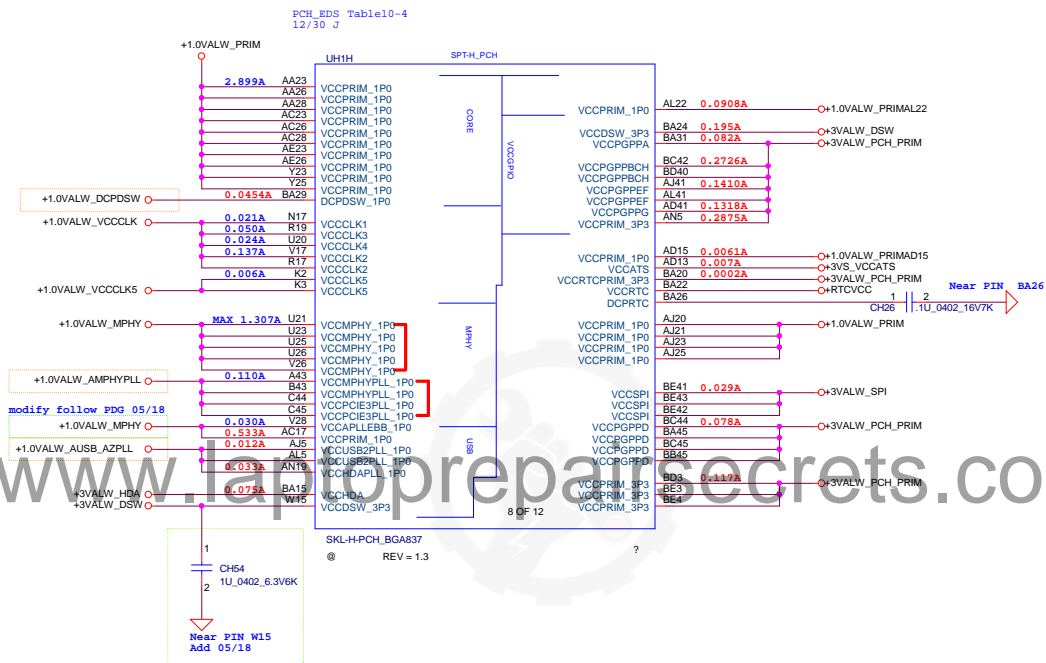
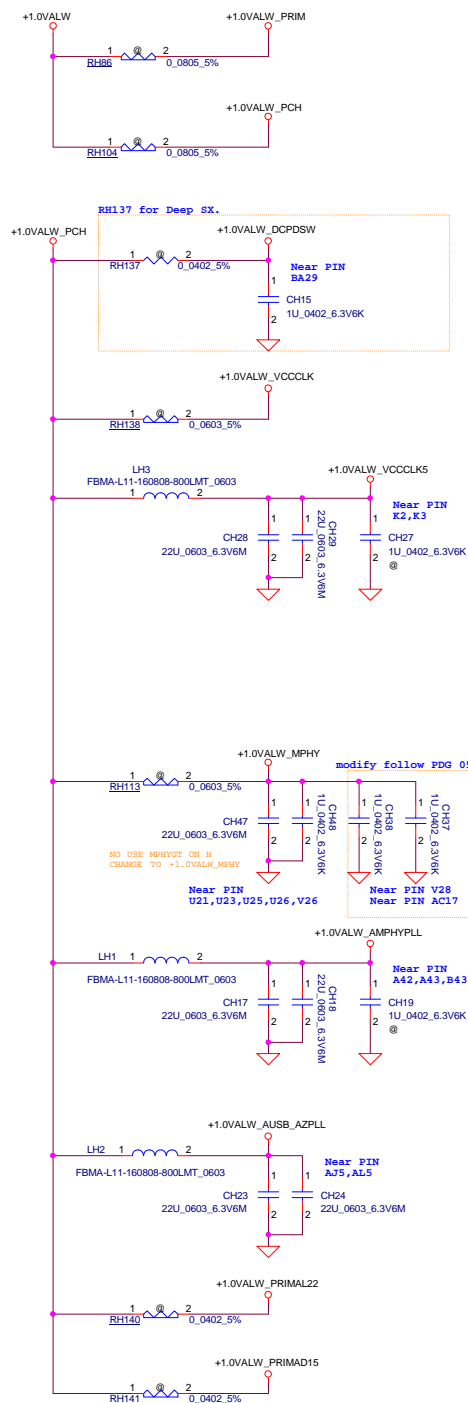


VGA_ID	GPP_D9
SGT	0
VGM	1

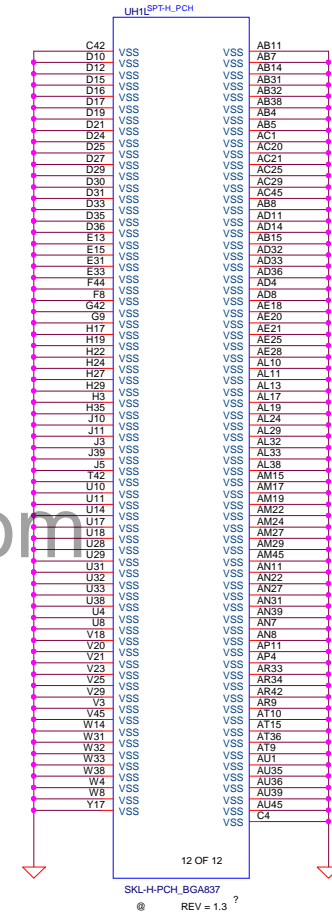
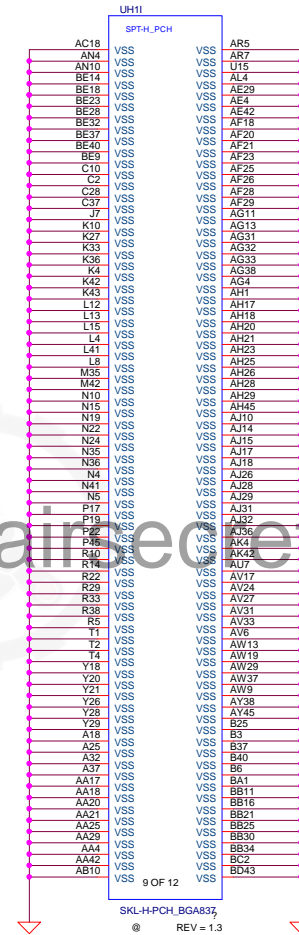
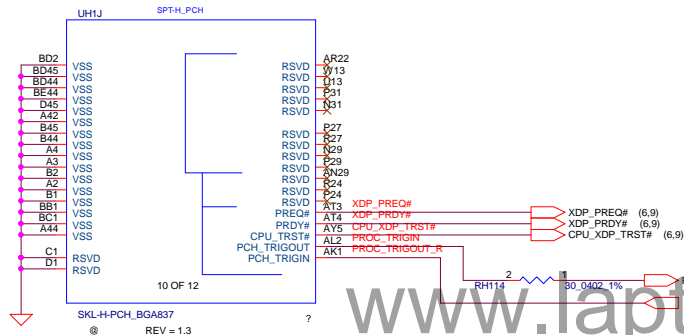
RANK_ID	GPP_D10
DR	0
SR	1

Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
* A4WAD	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1





Power Rail	Voltage
+CHGRTC	3.383V(MAX)
BAT54C(VF)	240 mV
+3VL_RTC	3.143V
Result : Pass	









Decive ID : 0x1347

Decive ID : 0x1299

ZZZ

X7607 @

X76614BOL57

ZZZ

X7608 @

X76614BOL58

GM2G SAM-N 256M16GT2G SAM-N 256M16

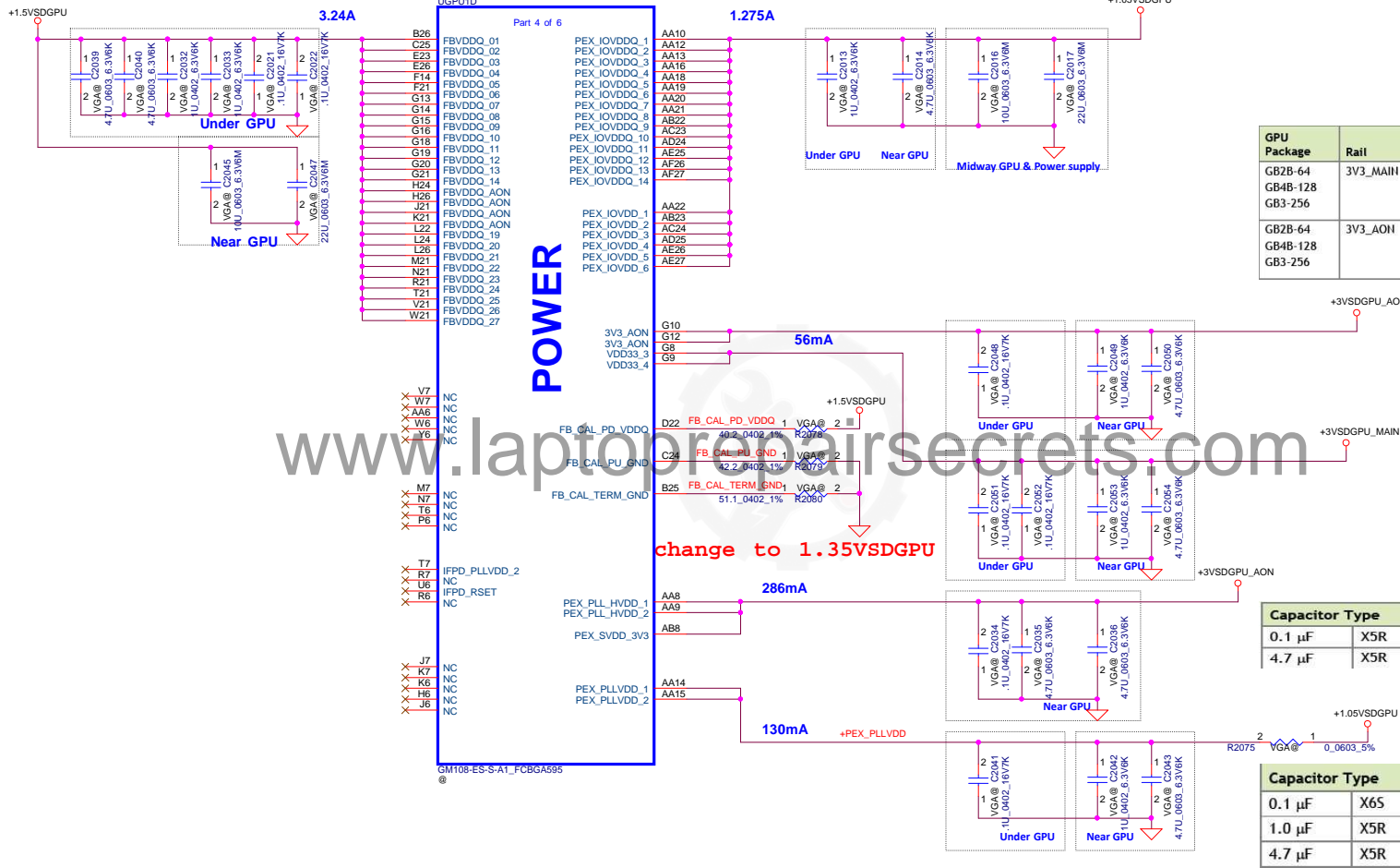
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.

NV 15x DG-06803-V03

GPU Package Type	Capacitor Type	Footprint		Population	Location	
GB2B-64 DDR3	0.1µF	X7R	0402	2	2	Under GPU
	1µF	X7R	0603	2	2	Under GPU
	4.7µF	X6S	0603	2	2	Under GPU
	10µF	X5R	0805	1	1	Near GPU
	22µF	X5R	0805	1	1	Near GPU

GPU Package Type	Capacitor Type		Footprint	Population	Location
GB2B-64	1.0 μF	X6S	0402	1	Under GPU
	4.7 μF	X6S	0603	1	Near GPU
	10 μF	X5R	0805	1	Midway between GPU and Power Supply
	22 μF	X5R	0805	1	Midway between GPU and Power Supply

change to 1.35VSDGPU

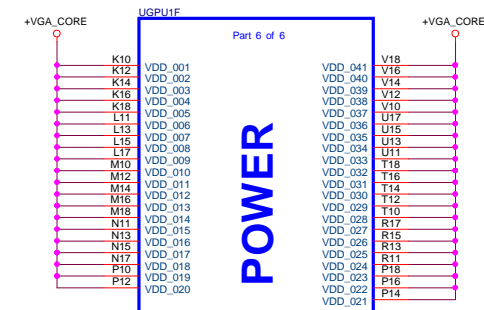
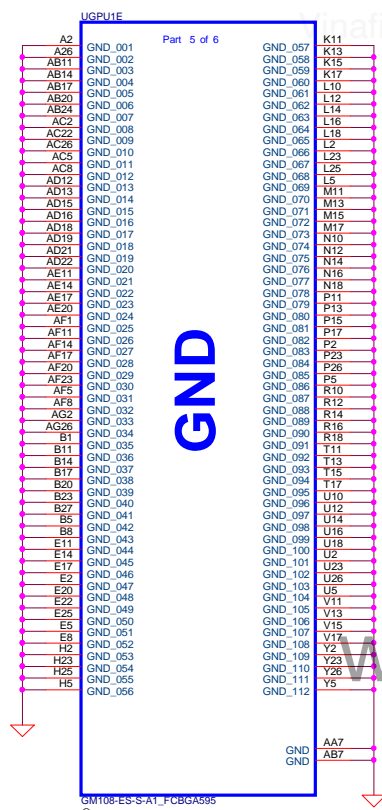


GPU Package	Rail	Capacitor Type		Footprint	Population		Location
GB2B-64 GB4B-128 GB3-256	3V3_MAIN	0.1µF	X6S	0402	2	2	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU
GB2B-64 GB4B-128 GB3-256	3V3_AON	0.1µF	X6S	0402	1	1	Under GPU
		1 µF	X5R	0603	1	1	Near GPU
		4.7 µF	X5R	0603	1	1	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X5R	0402	1	Near GPU
4.7 μF	X5R	0603	2	Near GPU

Capacitor Type		Footprint	Population	Location
0.1 μF	X6S	0402	1	Under GPU
1.0 μF	X5R	0603	1	Near GPU
4.7 μF	X5R	0805	1	Near GPU





### NV 15x DG-06803-V03

GPU Package Type	Capacitor Type		Footprint		Population	Location	Comments
GB2B-64	4.7 $\mu$ F	X6S	0603	10	10	Under GPU	
	1 $\mu$ F	X6S	0402	4	4	Under GPU	
	47 $\mu$ F	X5R	0805	1	1	Near GPU	
	22 $\mu$ F	X5R	0805	1	1	Near GPU	
	4.7 $\mu$ F	X5R	0805	5	5	Near GPU	
	330 $\mu$ F	POS	7343	1	1	Near GPU	ESR $\leq$ 6 m $\Omega$

### DA-06840-V03

Table 6. EDP-Peak

Products	VRM Type	GPU Core	FB Total	1.05V Total
		—	1.5/1.35V	1.05V
N155-GM	DDR3/L	48.11	4.23	0.91
N155-GT	DDR3/L	60.07	4.26	0.91

### DA-06925-V05

Table 6. EDP-Peak at  $T_j = 102^\circ\text{C}$

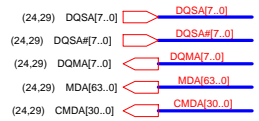
Power Supply Rail (V)	N15V-GM-S DDR3/L (A)
GPU Core Max	51.50
FB Total	4.25
PEXVDD	2.29

### DA07075-V01

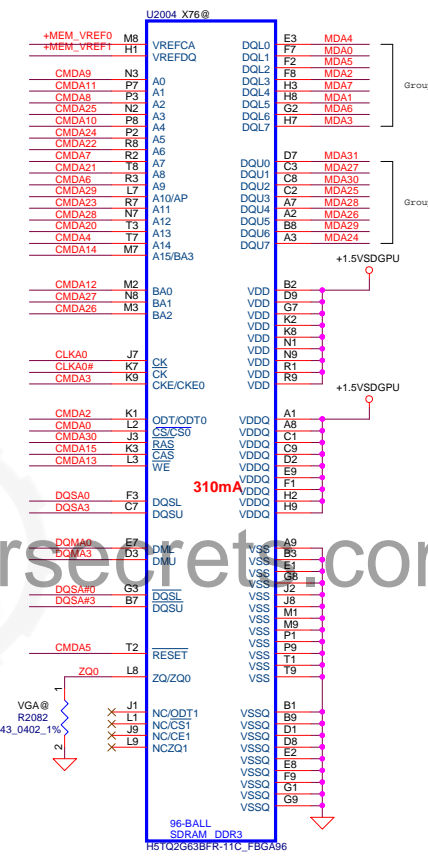
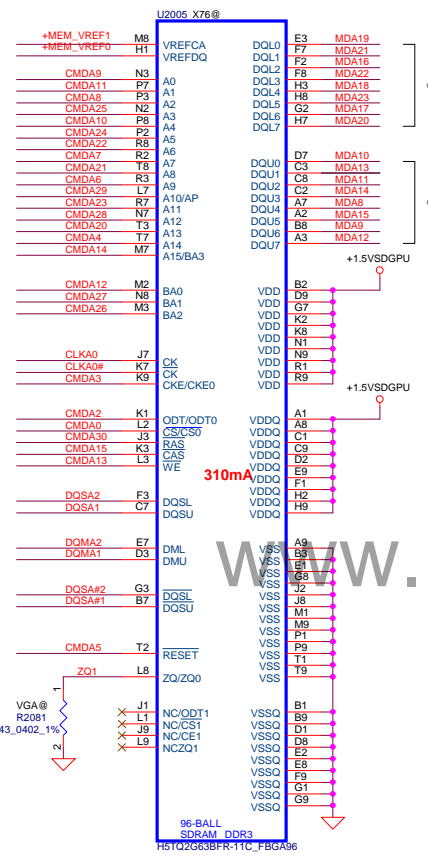
Table 7. EDP-Peak at  $T_j = 102^\circ\text{C}$

Power Supply Rail (V)	N15V-GL DDR3 (A)
GPU Core Max	28.26
FB Total	4.07
PEXVDD	1.82

VRAM DDR3 chips



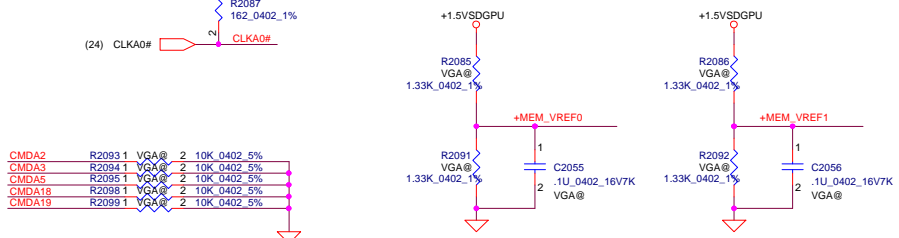
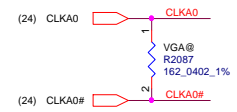
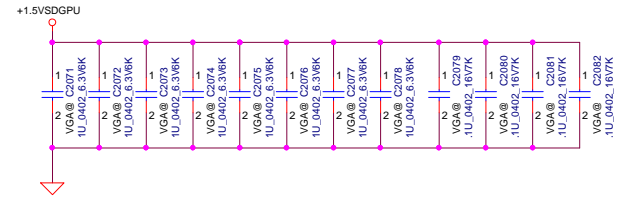
LOW BIT



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

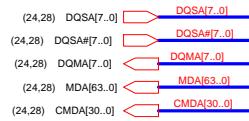
Table 3-11. DDR3 per Memory FBVDD/Q Decoupling

Capacitor Type		Population		Location
		FBVDDQ	FBVDD	
FBVDD/Q Combined				
0.1 µF	X7R	0402	2	Under DRAM
1.0 µF	X7R	0603	4	Under DRAM
10 µF	X5R	0805	0	Close to DRAM

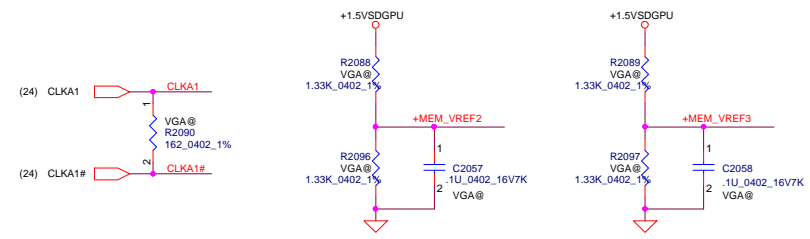
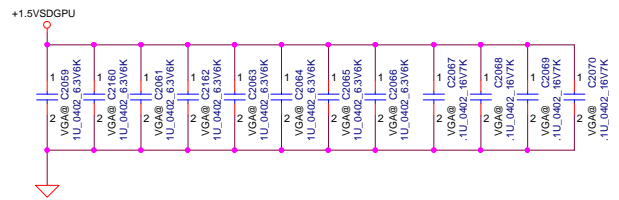
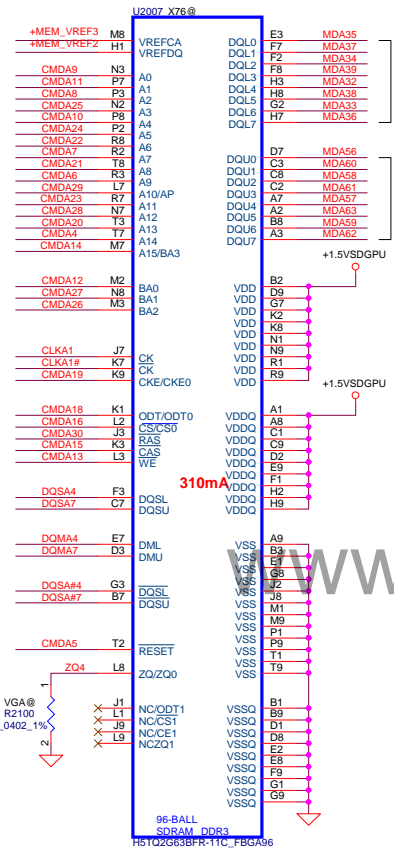


DDR3	Command Bit	Default Pull-down
	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

VRAM DDR3 chips



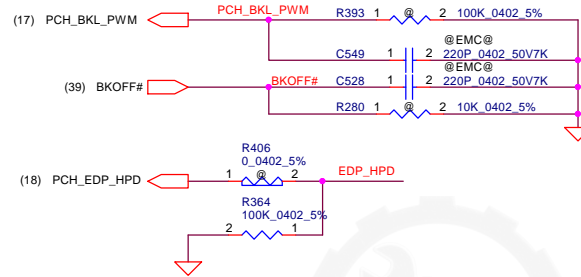
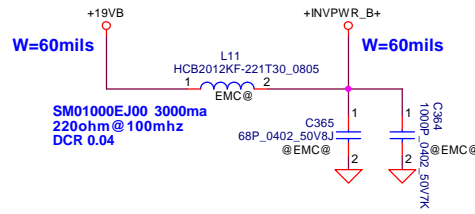
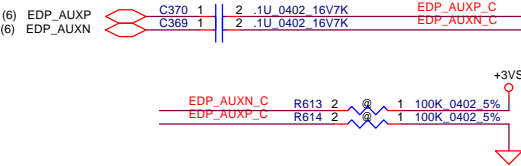
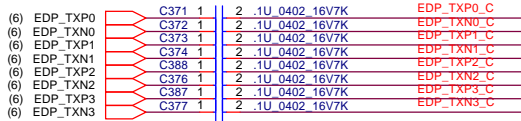
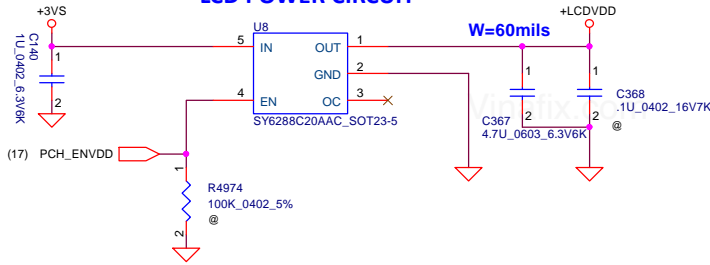
HIGH BIT



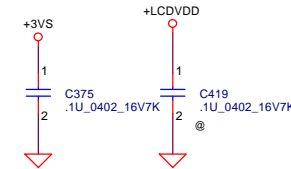
Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE_L	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		

Command Bit	Default Pull-down
ODTx	10k
CKEx	10k
RST	10k
CS*	No Termination

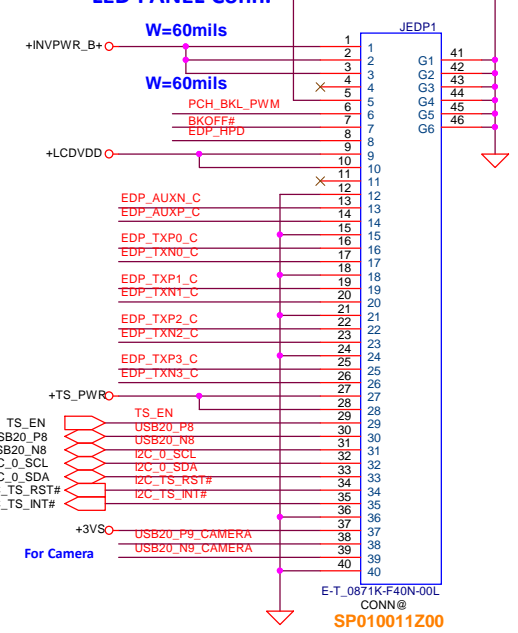
## LCD POWER CIRCUIT



## Place closed to JEDP1

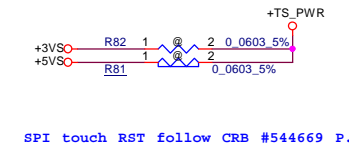


## LED PANEL Conn.

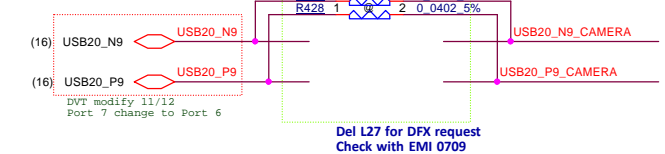


www.laptoprepairsecrets.com

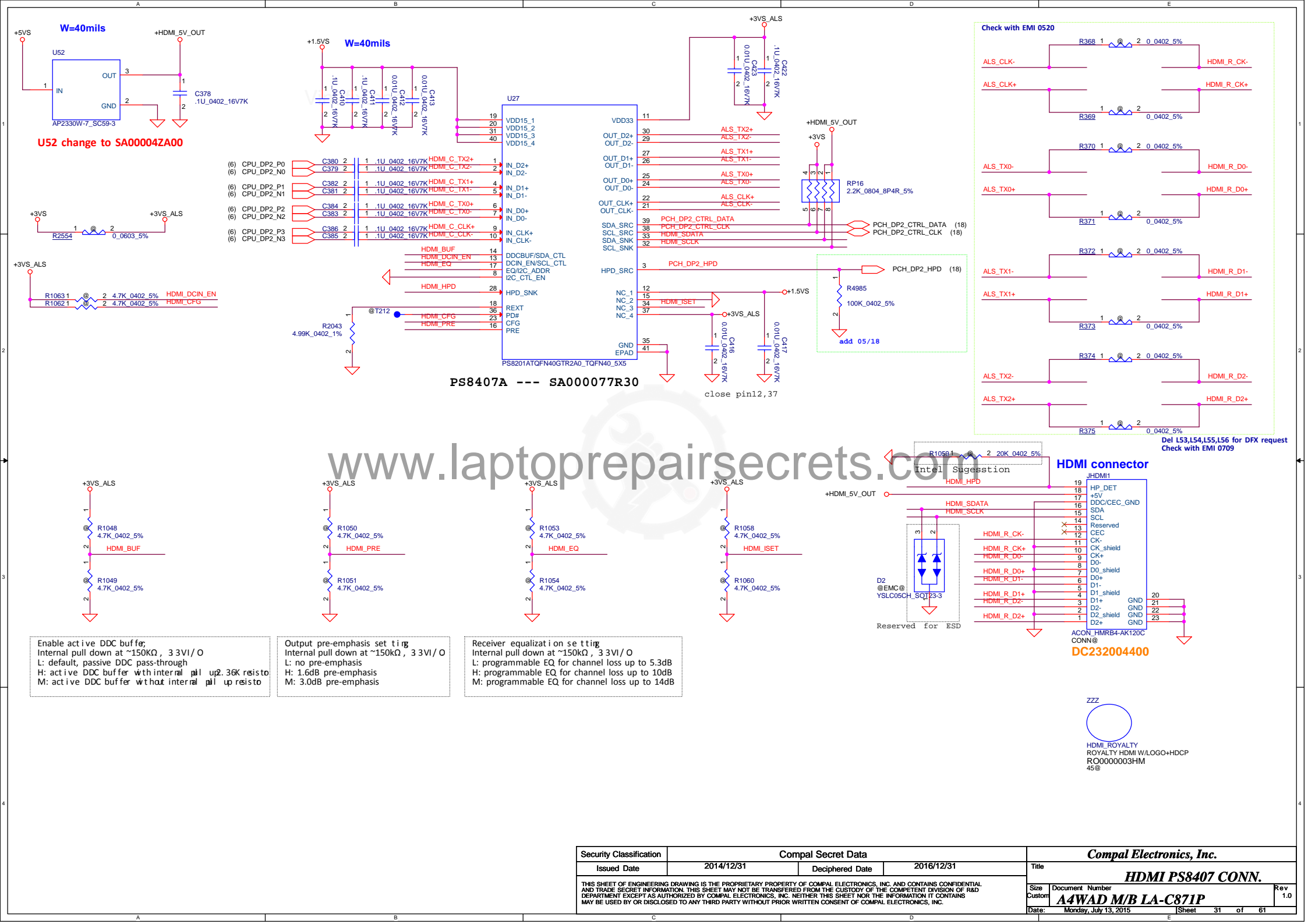
## I2C Touch Screen

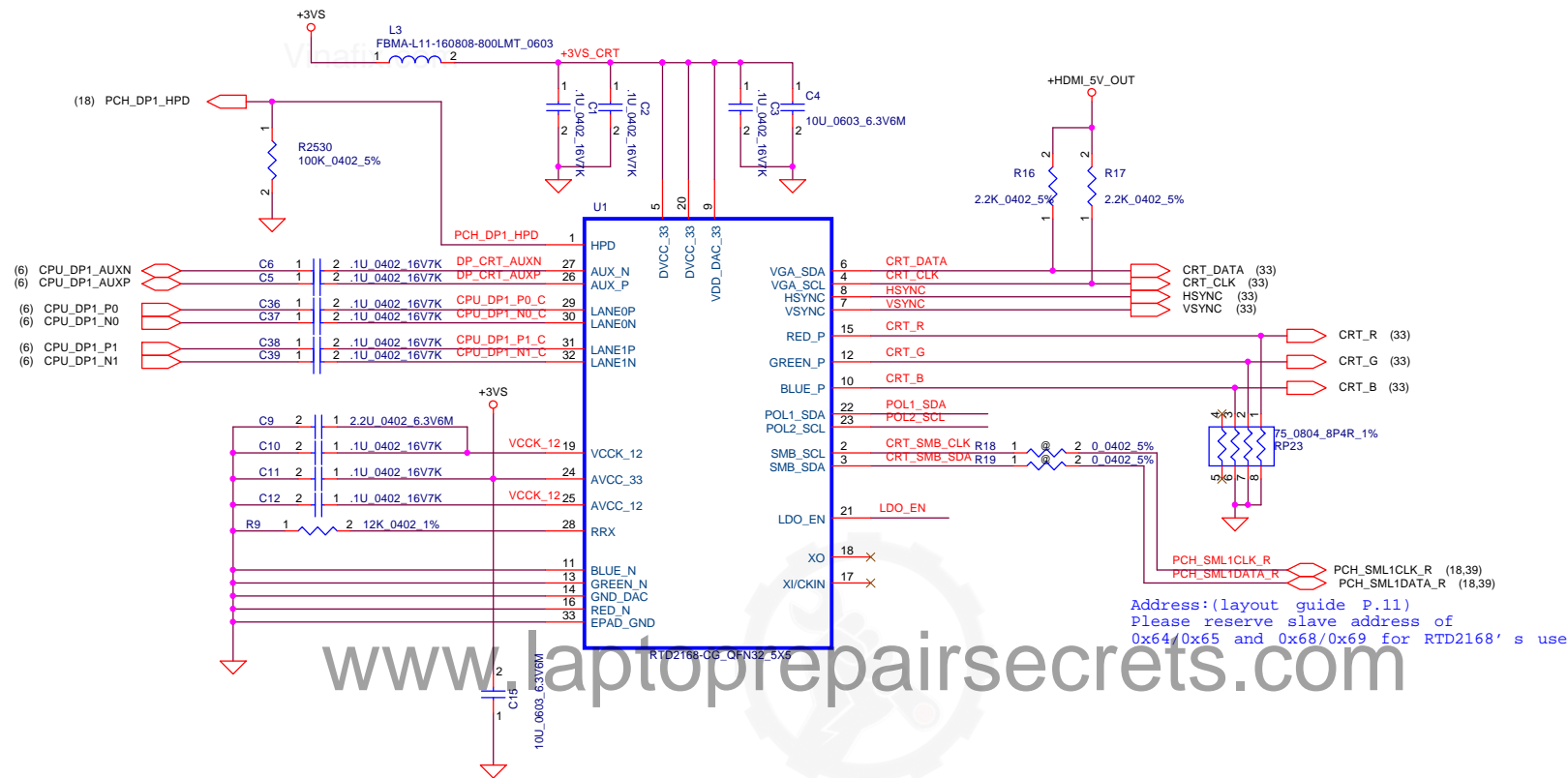


## Camera



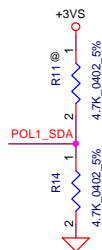
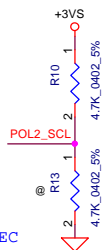
Security Classification		Compal Secret Data				Compal Electronics, Inc.							
Issued Date		2014/12/31		Deciphered Date		2016/12/31		Title					
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.								eDP CONN.					
								Size Custom		Document Number		Rev 1.0	
								Date: Monday, July 13, 2015		Sheet 30 of 61			
								A4WAD M/B LA-C871P					





		POL_SDA	
POL_SCL	0	X	EP
	1	*ROM	EEPROM

ROM: Internal ROM  
EP: Programmed external EC  
EEPROM: External ROM



LDO\_EN:  
\*1: Internal 1.2V  
0: External 1.2V

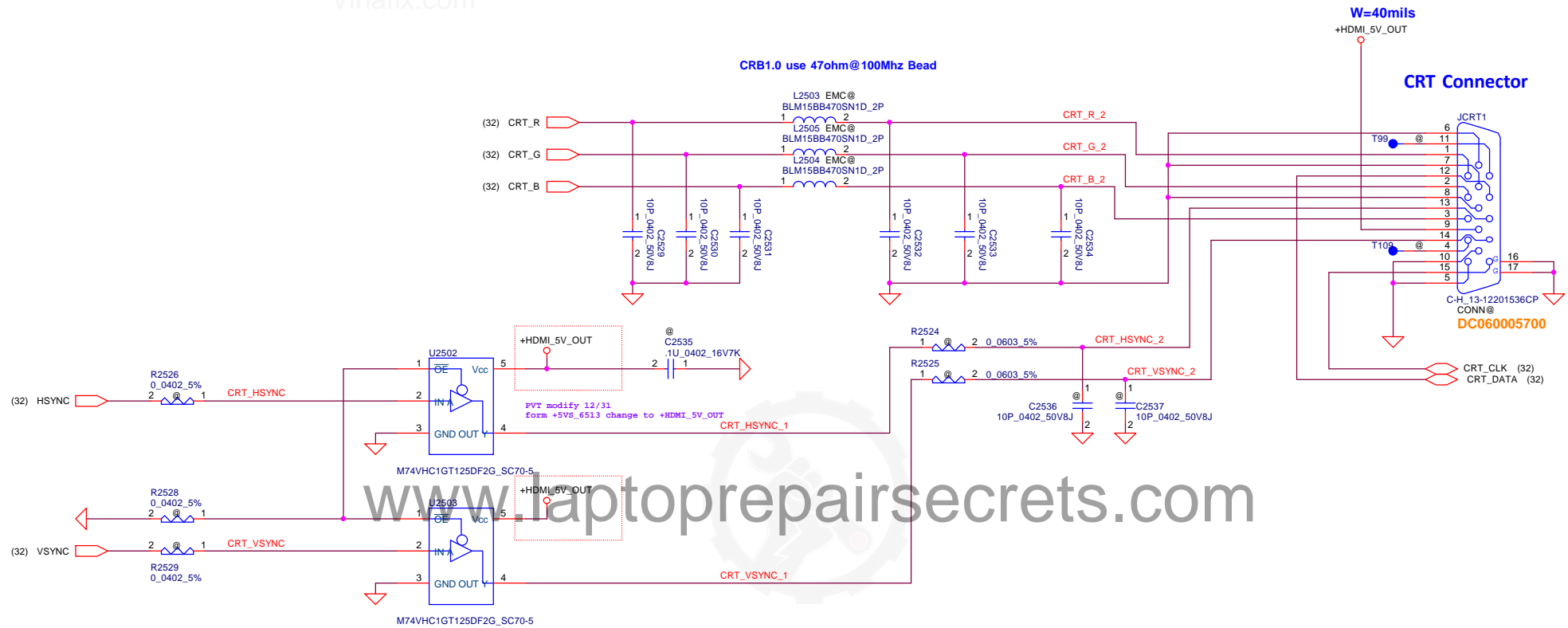
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				CRT Realtek RTD2168	
Size	Custom	Document Number	A4WAD M/B LA-C871P	Rev	1.0
Date:	Monday, July 13, 2015	Sheet	32	of	61



# CRT conn.

Vinafix.com

CRB1.0 use 47ohm@100Mhz Bead

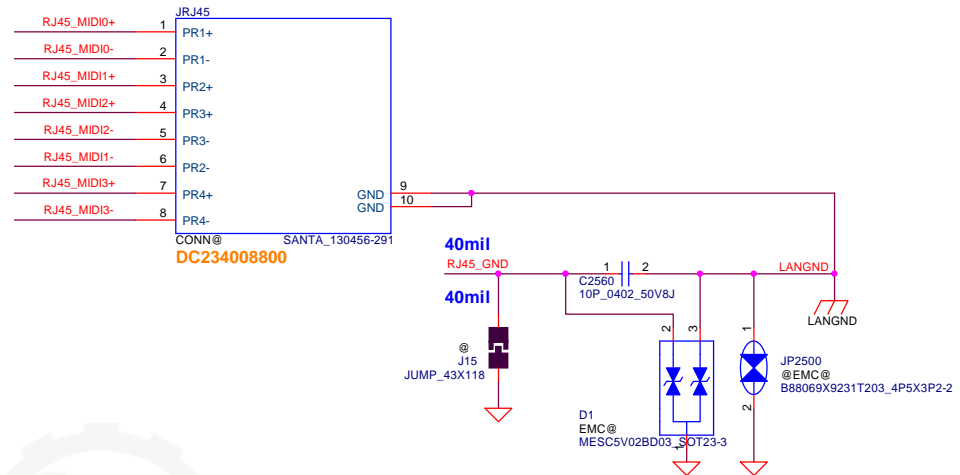
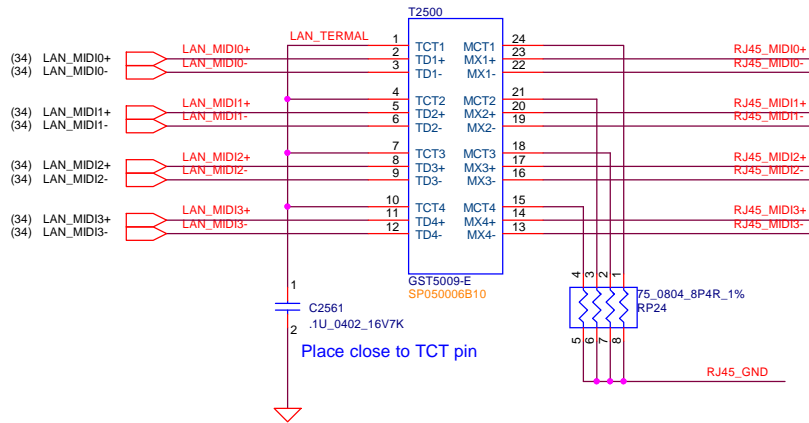


Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2014/12/31		Deciphered Date		2016/12/31		Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						CRT Connector					
						Size Custom		Document Number		Rev 1.0	
						Date: Monday, July 13, 2015		Sheet 33 of 61			
						A4WAD M/B LA-C871P					



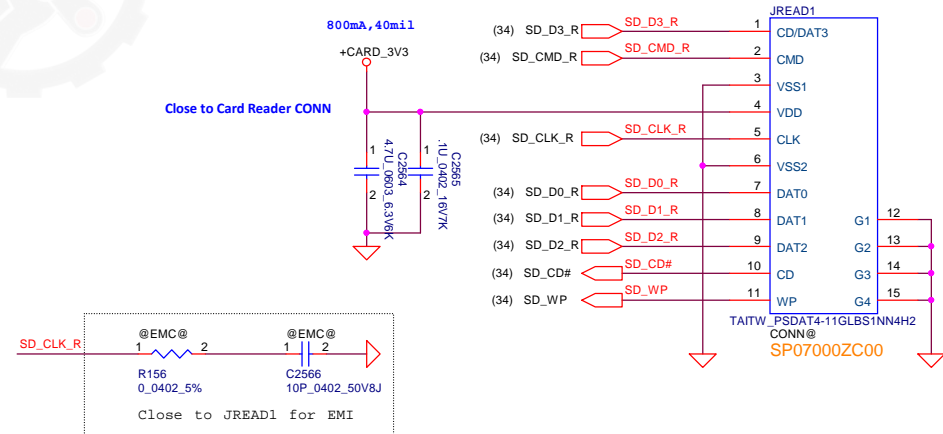
Vinafix.com

## LAN Connector



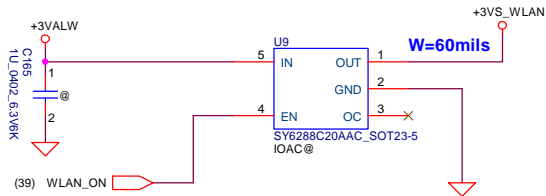
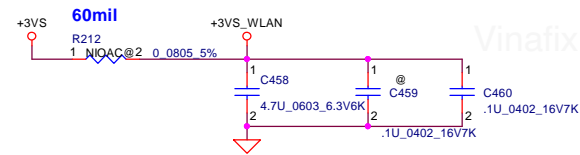
www.laptoprepairsecrets.com

## Card Reader Connector



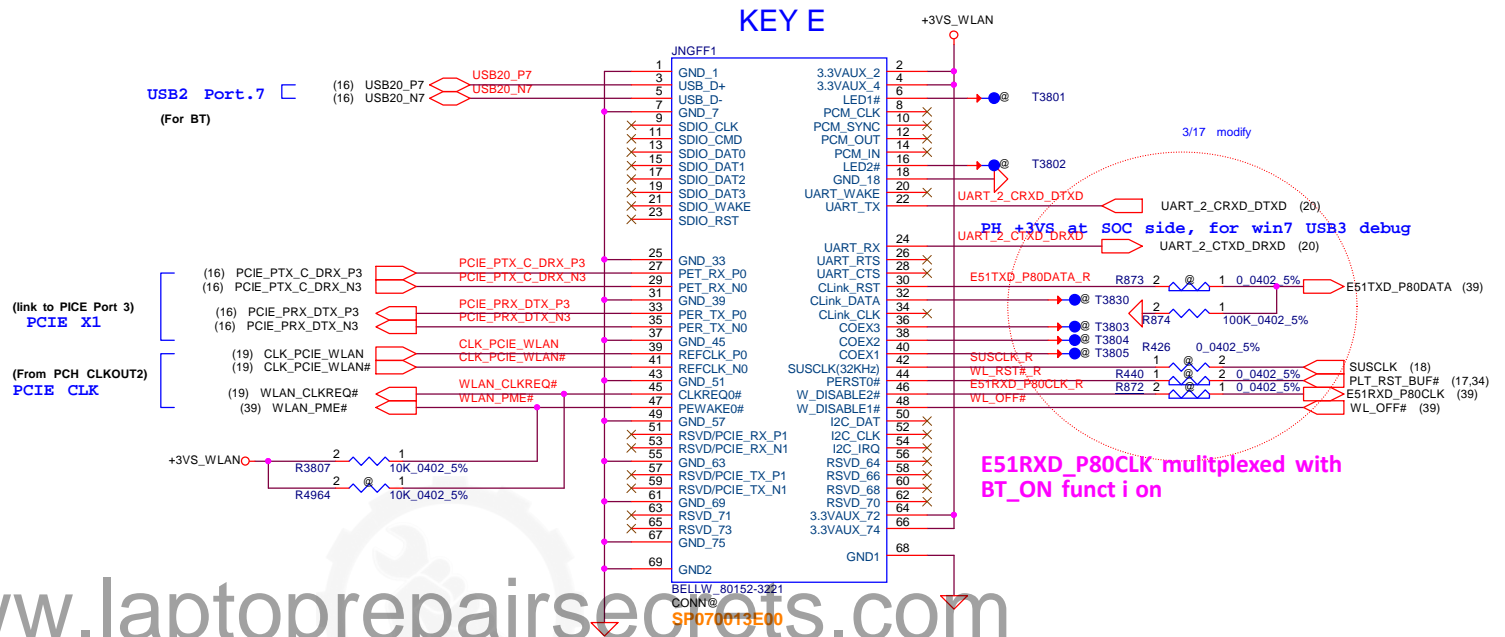
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				LAN RJ45/CR SD Connector		
				Size Document Number		
				A4WAD M/B LA-C871P		
				Rev 1.0		
				Date: Monday, July 13, 2015		
				Sheet 35 of 61		

# Wireless LAN



## NGFF WL+BT (KEY E)

74	3.3V	GND	75
72	3.3V	RESERVED/REFCLKN1	73
70	UM_Power_SRC/GPIO/PEWake1#	RESERVED/REFCLKP1	71
68	UM_Power_SRC/CLKREQ1#	GND	69
66	UM_SWP/PERST1#	Reserved/PERn1	67
64	RESERVED	Reserved/PERp1	65
62	ALERT# (IO/0/3.3)	GND	63
60	DC CLK (IO/0/3.3)	Reserved/PERnL	61
58	DC DATA (IO/0/3.3)	Reserved/PERp1	59
56	W_DISABLE#1 (O/0/3.3V)	GND	57
54	Reserved_W_DISABLE#2 (O/0/3.3V)	PEWakeDr (IO/0/3.3V)	55
52	PERST0# (IO/0/3.3V)	CLKREQDr (IO/0/3.3V)	53
50	SUSCLK(32KHz) (O/0/3.3V)	GND	51
48	CODEX1 (IO/0/1.8V)	REFCLKN0	49
46	CODEX2 (IO/0/1.8V)	REFCLKP0	47
44	CODEX3 (IO/0/1.8V)	GND	45
42	VENDOR DEFINED	PERn0	43
40	VENDOR DEFINED	PERp0	41
38	VENDOR DEFINED	GND	39
36	UART RTS (IO/0/1.8V)	PERn0	37
34	UART CTS (IO/0/1.8V)	PERp0	35
32	UART Tx (IO/0/1.8V)	GND	33
30	SDIO_RESET# (IO/0/1.8V)	SDIO_CLK (O/0/1.8V)	29
28	SDIO_WAKE# (IO/0/3.3V)	SDIO_CMD (O/0/1.8V)	27
26	GND	SDIO_DAT0 (O/0/1.8V)	25
24	LED#1 (IO/0/1.8V)	SDIO_DAT1 (O/0/1.8V)	23
22	PCM_OUT/IO/SD_OUT (O/0/1.8V)	SDIO_DAT2 (O/0/1.8V)	21
20	PCM_IN/IO/SD_IN (IO/0/1.8V)	SDIO_DAT3 (O/0/1.8V)	19
18	PCM_SYNC/IO/SD_IN (IO/0/1.8V)	SDIO_CMD (O/0/1.8V)	17
16	PCM_CLK/IO/SD_IN (IO/0/1.8V)	SDIO_CLK (O/0/1.8V)	15
14	LED#1 (IO/0/1.8V)	GND	13
12	3.3V	USB_D-#	11
10	3.3V	USB_D-#	9
8	3.3V	GND	7
6	3.3V	GND	5
4	3.3V	GND	3
2	3.3V	GND	1



www.laptoprepairsecrets.com

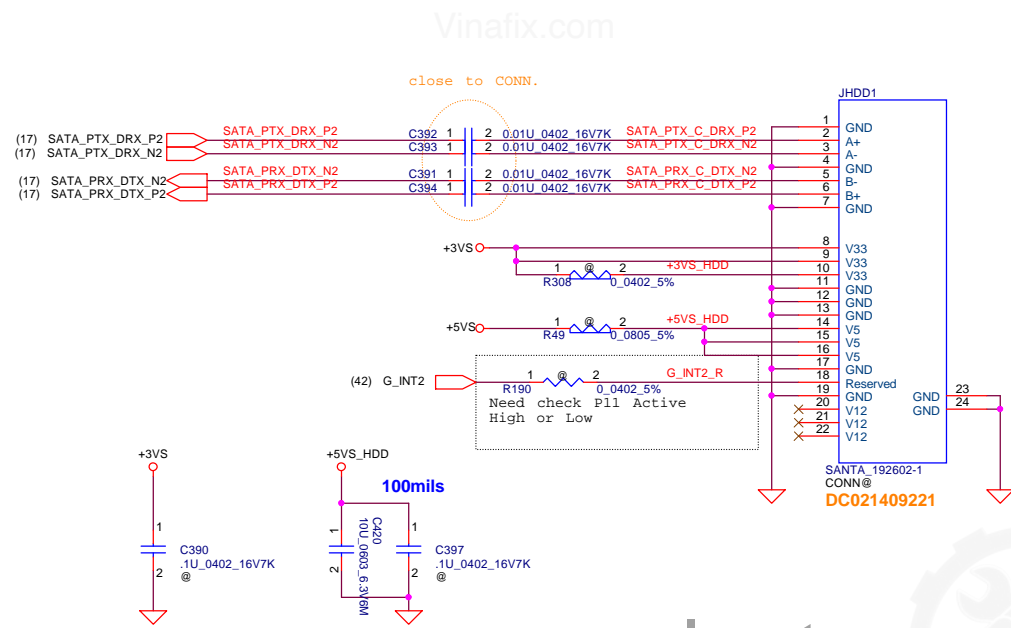
### 3.4-8.4-3.1.7.1. UART Wakeup

The UART power management protocol supports the following 4-wire and 5-wire interfaces:

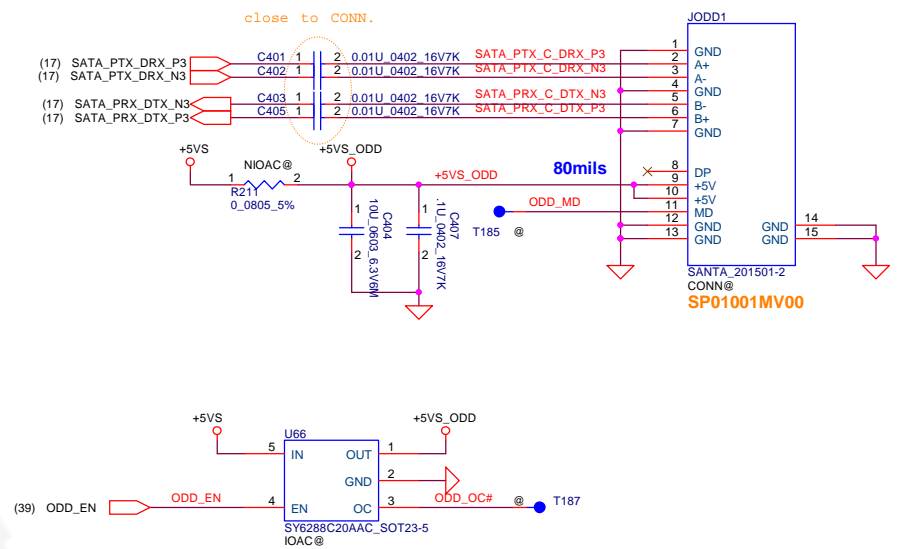
- ☐ ~~RDX~~ **UART\_RXD** (Input): Receive Data
- ☐ ~~RTX~~ **UART\_TXD** (Output): Transmit Data
- ☐ **UART\_RTS** (Input): Request to Send (Host Flow Control)
- ☐ **UART\_CTS** (Output): Clear to Send (Device Flow Control)
- ☐ **Host Wake-Up/UART\_Wake#** (Output): Host wake-up line is optional in case the host support in band wake-up

Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title					
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				M.2 Key E (WLAN)					
				Size	Document Number			Rev	
				Custom	A4WAD M/B LA-C871P			1.0	
				Date:	Monday, July 13, 2015		Sheet	36	of 61

SATA HDD Conn.

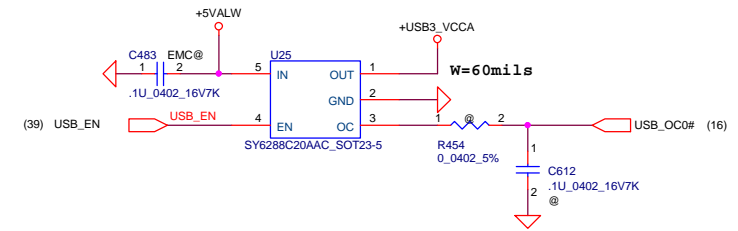
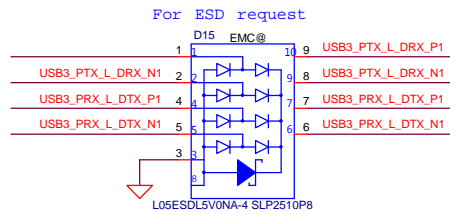
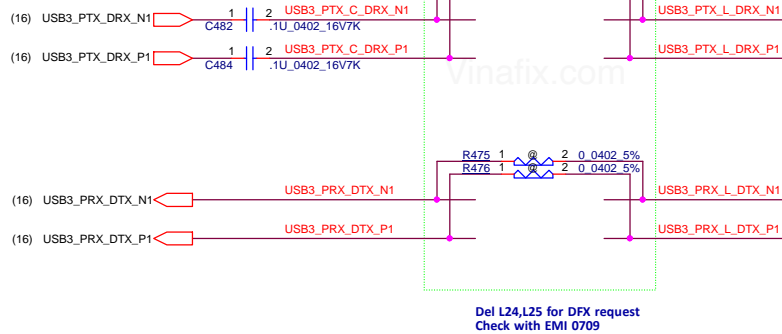


SATA ODD Conn.

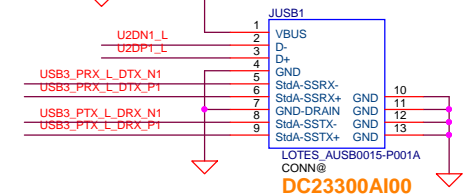


www.laptoprepairsecrets.com

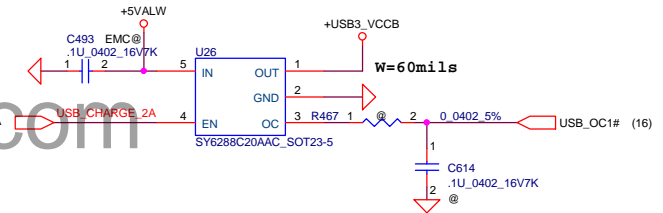
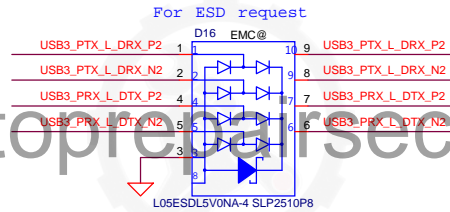
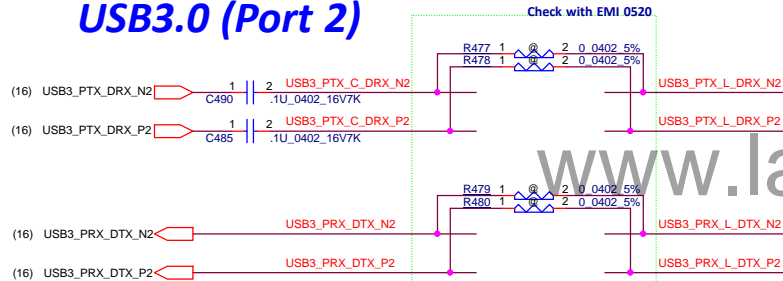
## USB3.0 (Port 1)



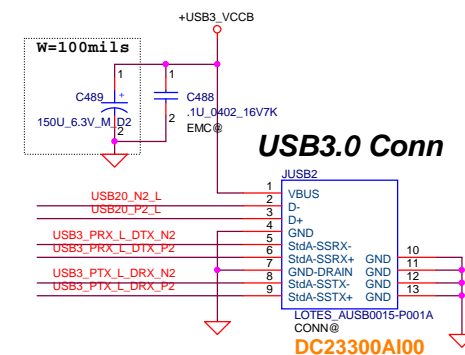
## USB3.0 Conn.



## USB3.0 (Port 2)



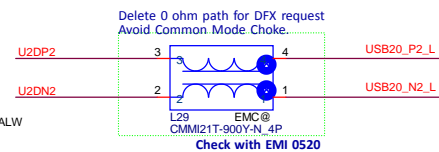
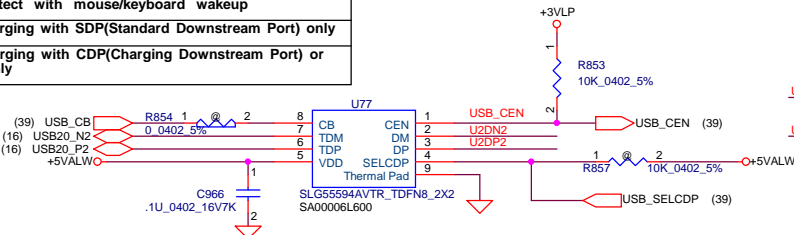
## USB3.0 Conn



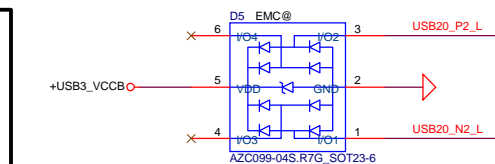
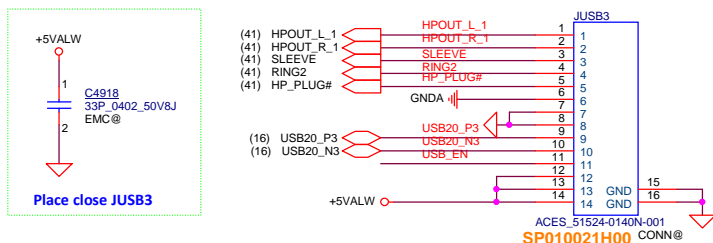
## USB Host Charger

CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only

Del L28, L30 for DFX request  
Check with EMI 0709

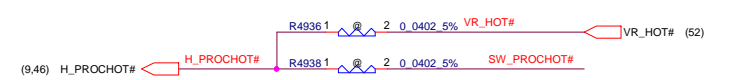
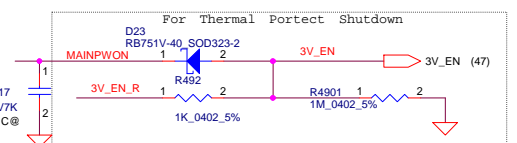
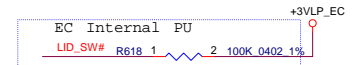
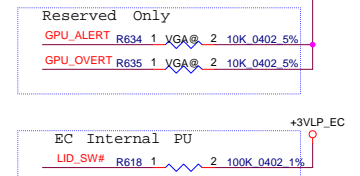
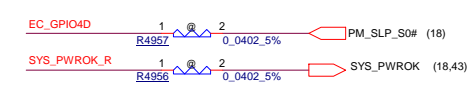
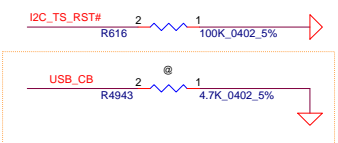
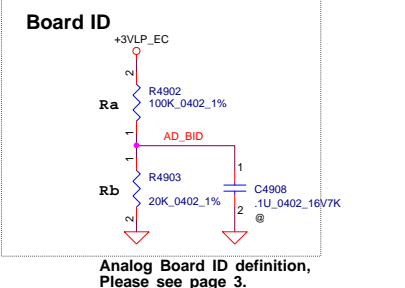
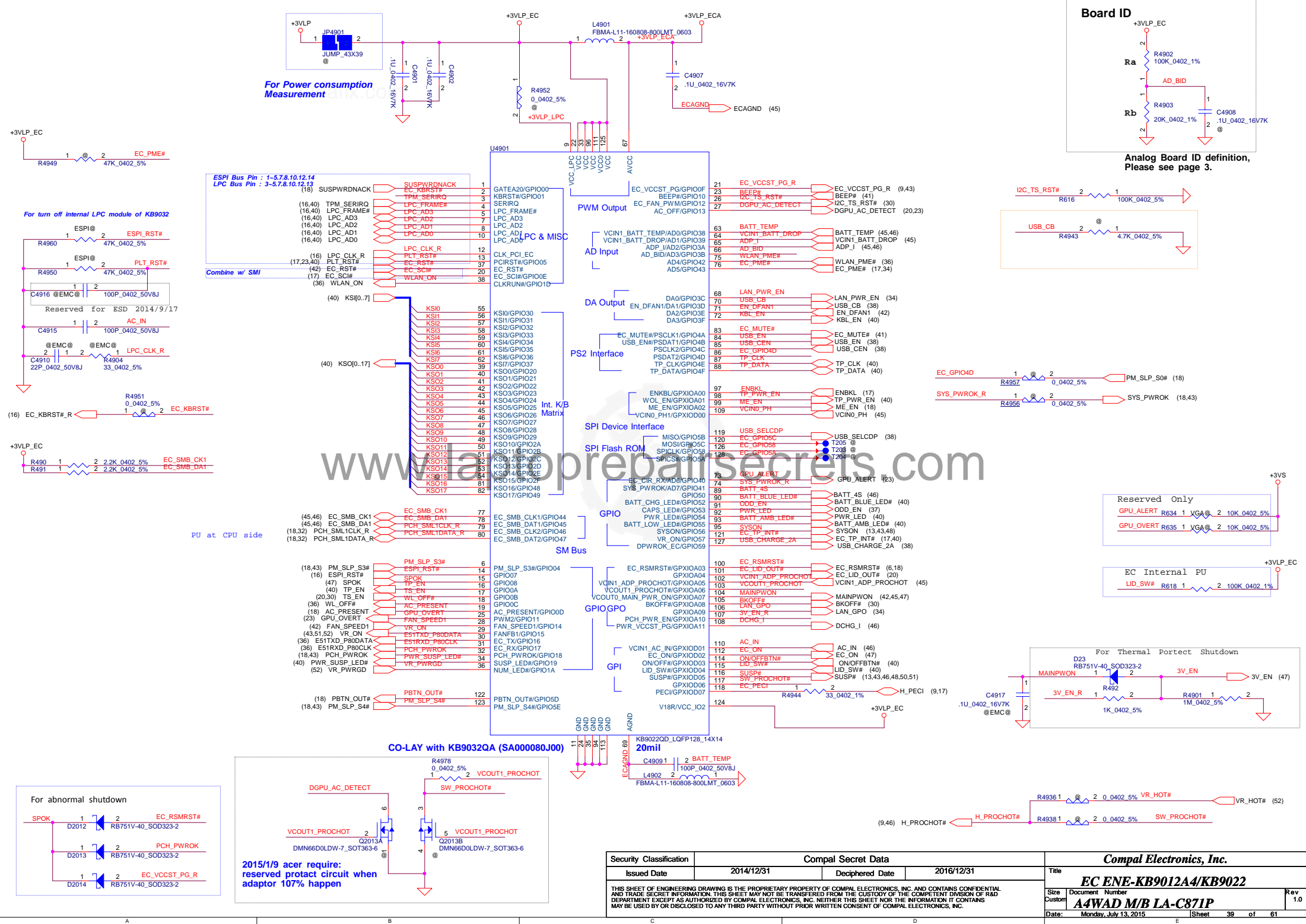


## USB/B (USB Port 3, + AUDIO)



Security Classification				Compal Secret Data		Compal Electronics, Inc.	
Issued Date		Deciphered Date		Title		USB3.0 Conn/USB B	
2014/12/31		2016/12/31		Size		A4WAD M/B LA-C871P	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.		Customer		Date		Rev	
				Monday, July 13, 2015		1.0	
				Sheet		38 of 61	





Security Classification				Compal Secret Data				Compal Electronics, Inc.		
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	EC ENE-KB9012A4/KB9022					
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev				
				Custom	A4WAD M/B LA-C871P	1.0				
				Date	Monday, July 13, 2015	Sheet	39	of 61		

**TP/B Conn.**

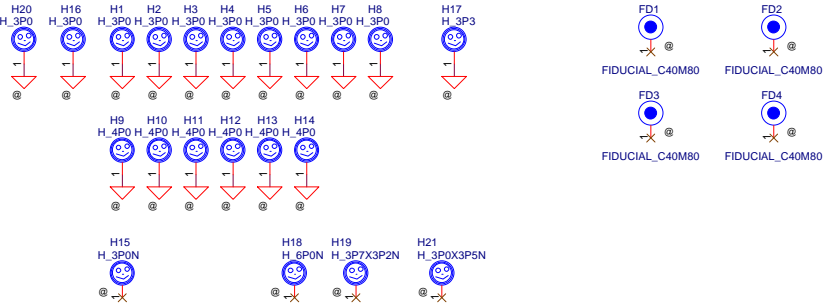
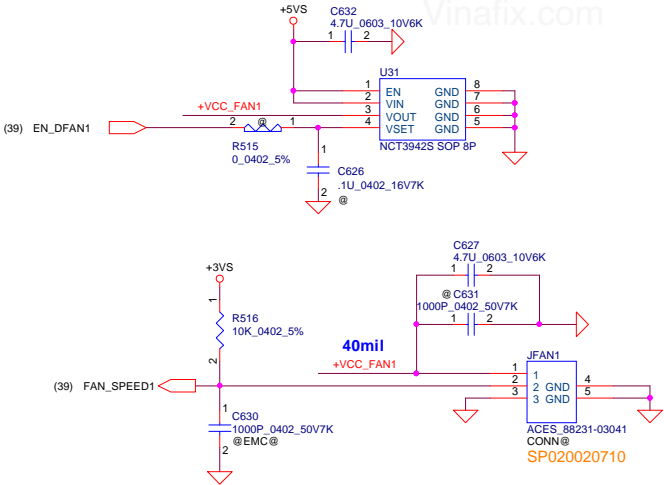


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RAD DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<b>KB &amp; TP &amp; TPM Connector &amp; LED</b>		
				Size	Document Number	Rev
				Custom	<b>A4WAD M/B LA-C87IP</b>	1.0
Date:	Monday, July 13, 2015	Sheet	40	of	61	



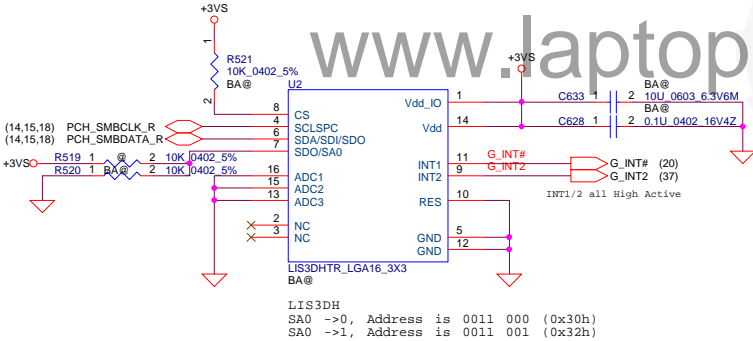
FAN1 Conn

Screw Hole

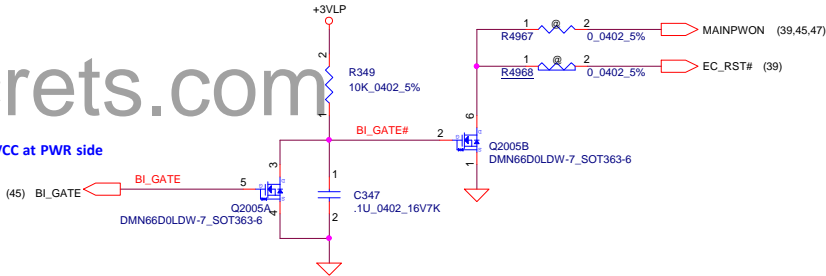


G-Sensor reserved for BA serial

Reset Circuit

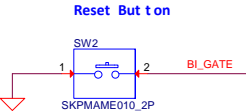


BI\_GATE PH to +RTCVCC at PWR side

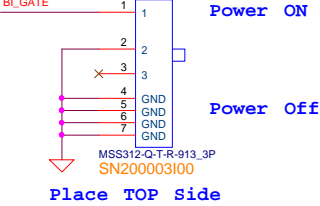


Debug SW

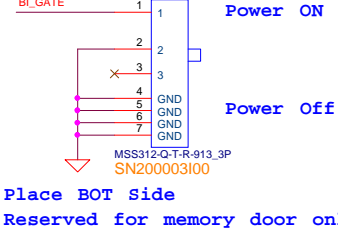
Reset But t on



BI SW

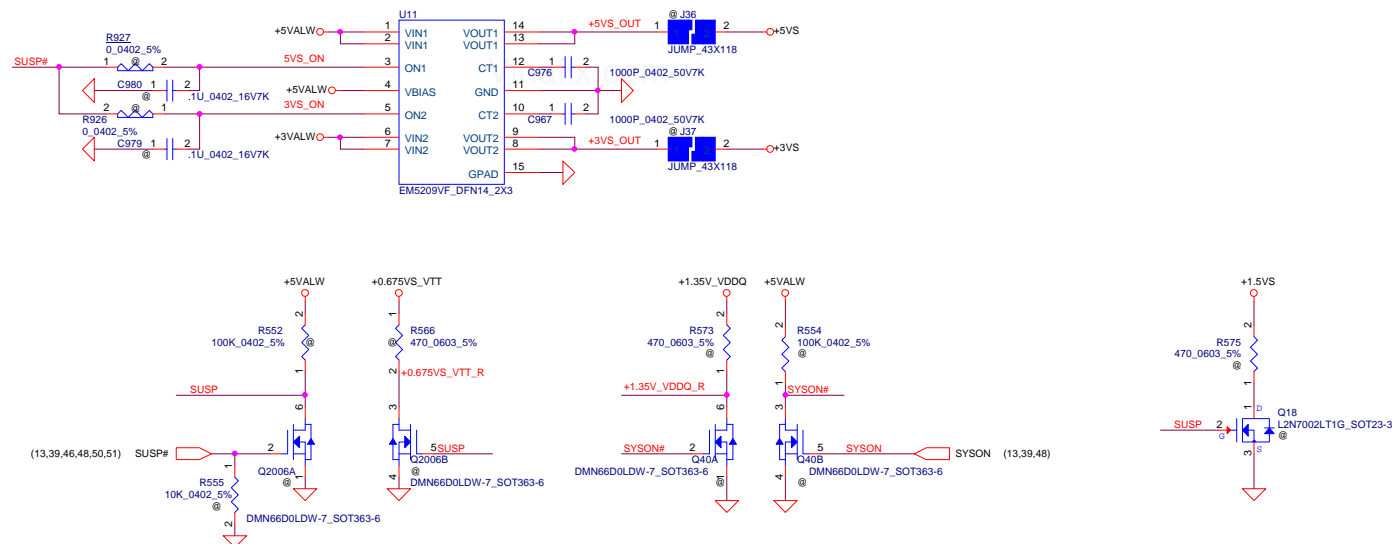


BI SW



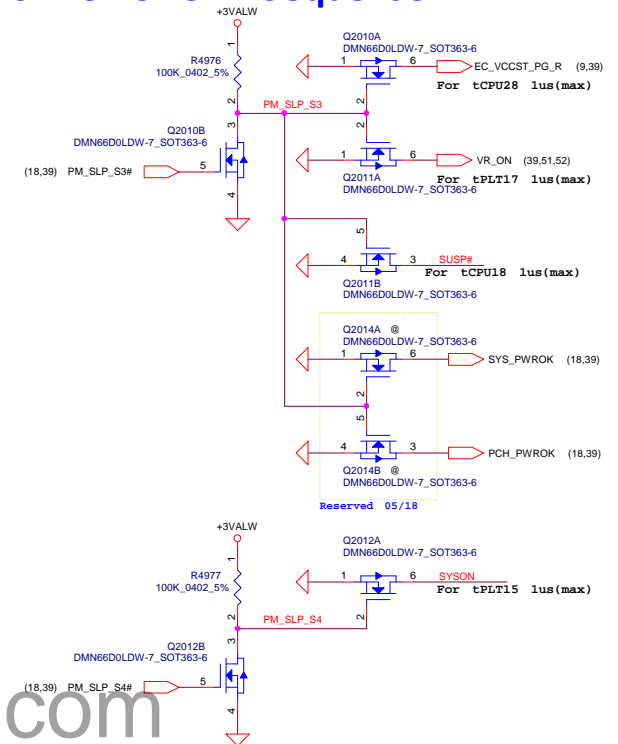
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				FAN & Screw Hole & G-Sensor		
Size	Document	Number		Rev		
Custom	A4WAD M/B LA-C871P			1.0		
Date:	Monday, July 13, 2015	Sheet	42	of	61	

## DC & VGA Interface

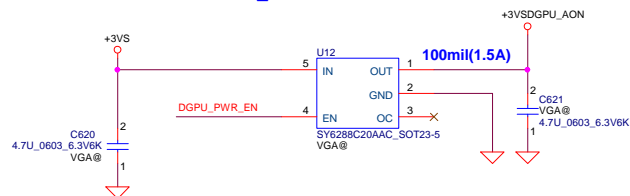


www.laptoprepairsecrets.com (18:39) PM SLP S44 

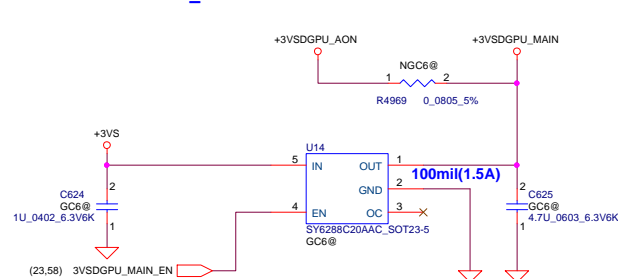
### For Power Of f Sequence



**+3VS to +3VSDGPU\_AON for GPU**



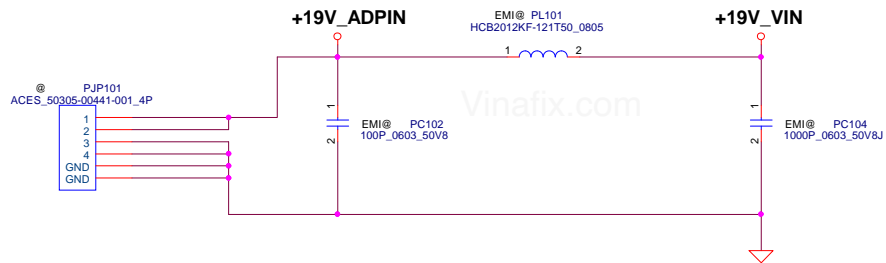
**+3VS to +3VSDGPU\_MAIN for GC6-2.0**



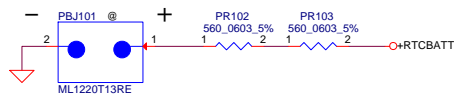
3VSDGPU\_MAIN\_EN From GPU



Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date		2014/12/31	Deciphered Date	2016/12/31	Title				
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					DC Interface				
					Size	Document Number		Rev	
						A4WAD M/B LA-C871P		1.0	
Date:					Monday, July 13, 2015	Sheet	43	of	61

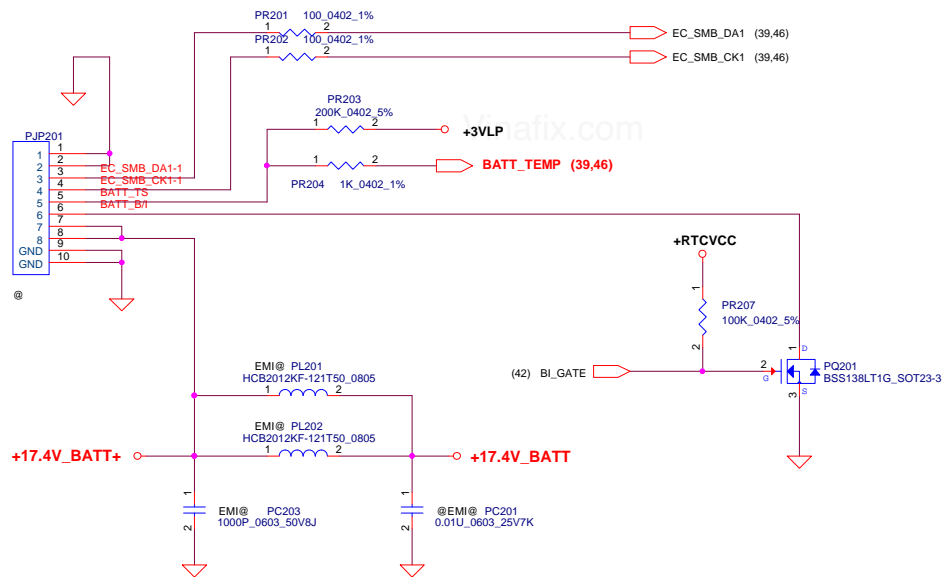


www.laptoprepairsecrets.com

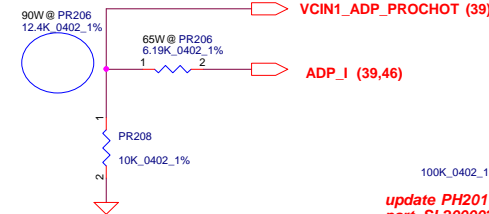


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	<b>PWR DCIN / Pre-charge</b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	<b>A4WAD M/B LA-C871P</b>
				Date:	Monday, July 13, 2015
				Sheet	44 of 61
				Rev	1.0



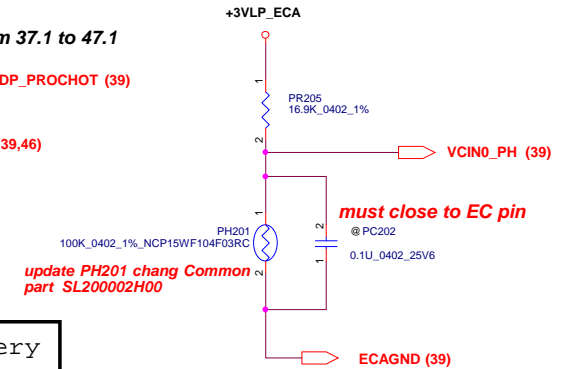


2013/07/23  
change PC5 and PC6 function field from 37.1 to 47.1



For KB9022 sense 20mΩ	Active	Recovery
65W PR206 6.19K ohm	84.5W, 0.54V	65W, 0.42V
90W PR206 12.4K ohm	117W, 0.54V	90W, 0.42V

PH1 under CPU bottom side :  
CPU thermal protection at 93 +-3 degree C  
Recovery at 56 +-3 degree C

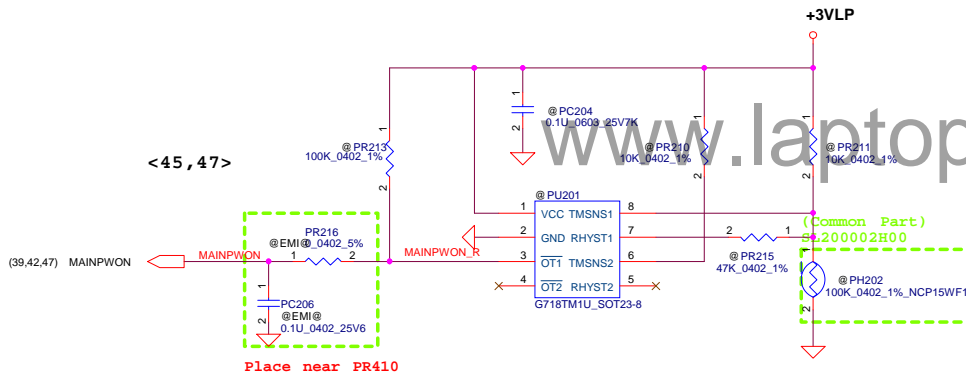


For 65W adapter====>action 84.5W, recovery 65W  
65W:  
Iada=0~3.42A (65W/19v=3.42A)  
ADP\_I=20\*Iada\*Rsense  
=20\*3.42\*0.01=0.6842V  
VCIN1\_PROCHOT=0.6842\*10/(10+x)=0.42V  
PR206=x=6.291k ohm

84.5W:  
Iada=0~4.447A (84.5W/19v=4.447A)  
ADP\_I=20\*Iada\*Rsense  
=20\*4.447\*0.01=0.8895V  
VCIN1\_PROCHOT=0.8895\*10/(10+x)=0.55V  
PR206=x=6.17k ohm

For 90W adapter====>action 117W, recovery 90W  
90W:  
Iada=0~4.737A (90W/19v=4.737A)  
ADP\_I=20\*Iada\*Rsense  
=20\*4.737\*0.01=0.9474V  
VCIN1\_PROCHOT=0.9474\*10/(10+x)=0.42V  
PR206=x=12.56k ohm

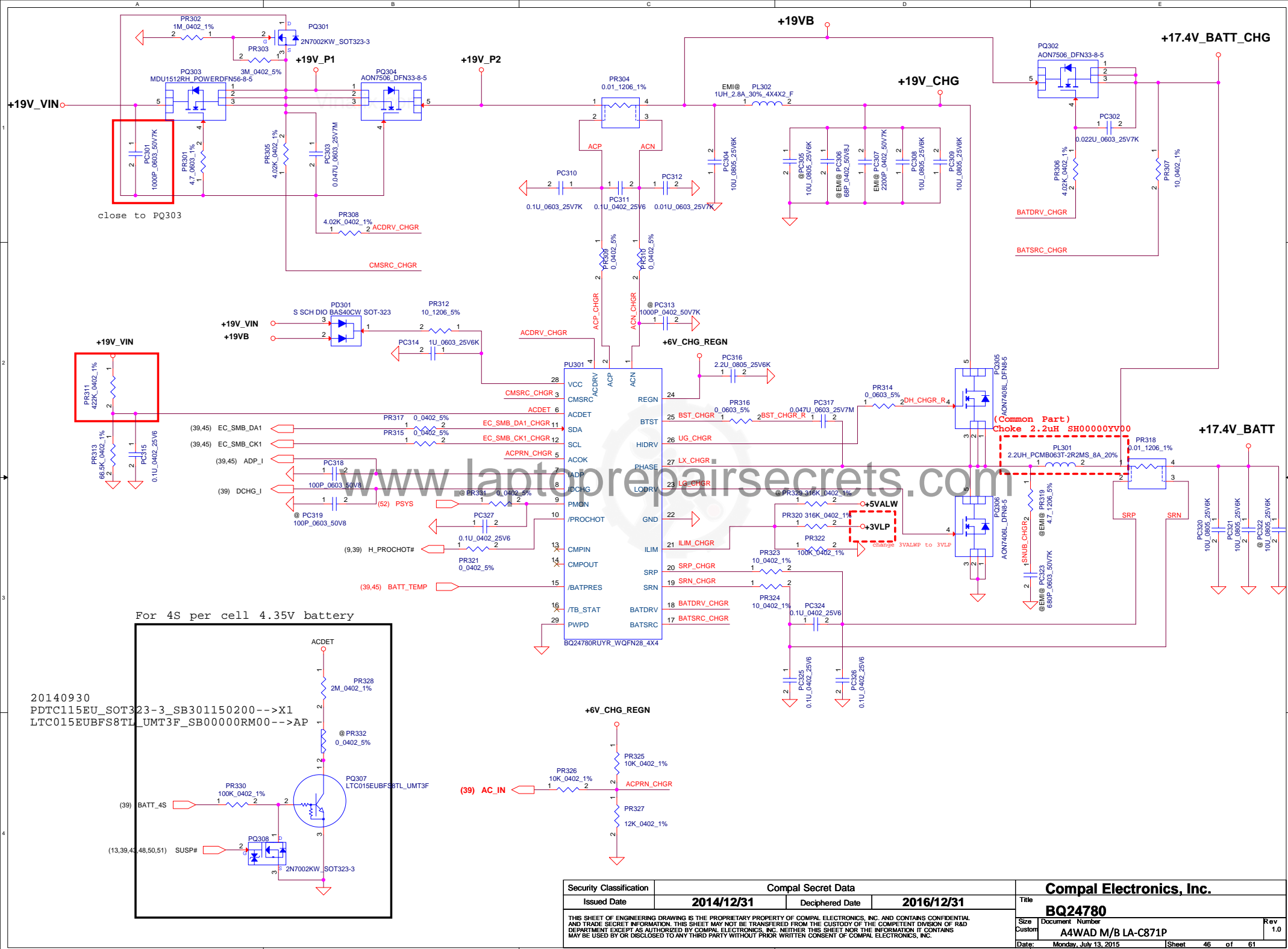
117W:  
Iada=0~6.158A (117W/19v=6.158A)  
ADP\_I=20\*Iada\*Rsense  
=20\*6.158\*0.01=1.232V  
VCIN1\_PROCHOT=1.232\*10/(10+x)=0.55V  
PR206=x=12.39k ohm



2013/06/07  
Add for ENE9022 Battery Voltage drop detection.  
Connect to ENE9022 pin64 AD1.

VAL50/ZAL20 Battery is 3-cell NVDC design.  
B+=9V  
Change PR12=50k if Battery is 2-cell NVDC design  
B+=6V

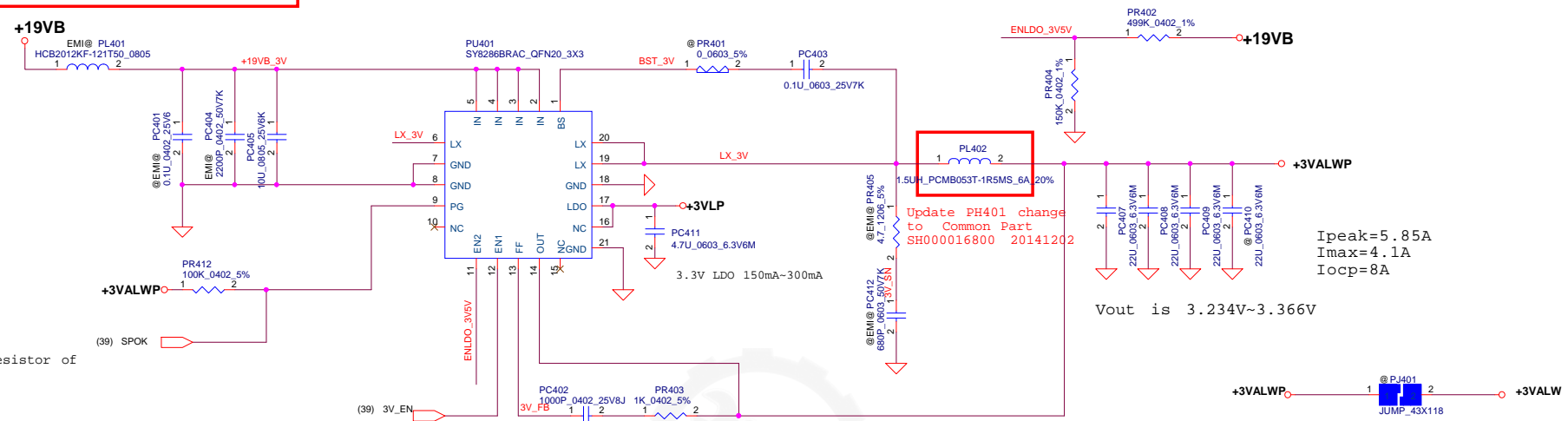
Security Classification	Compal Secret Data		Title	
Issued Date	2014/12/31	Deciphered Date	2016/12/31	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev 1.0
Date: Monday, July 13, 2015				Sheet 45 of 61



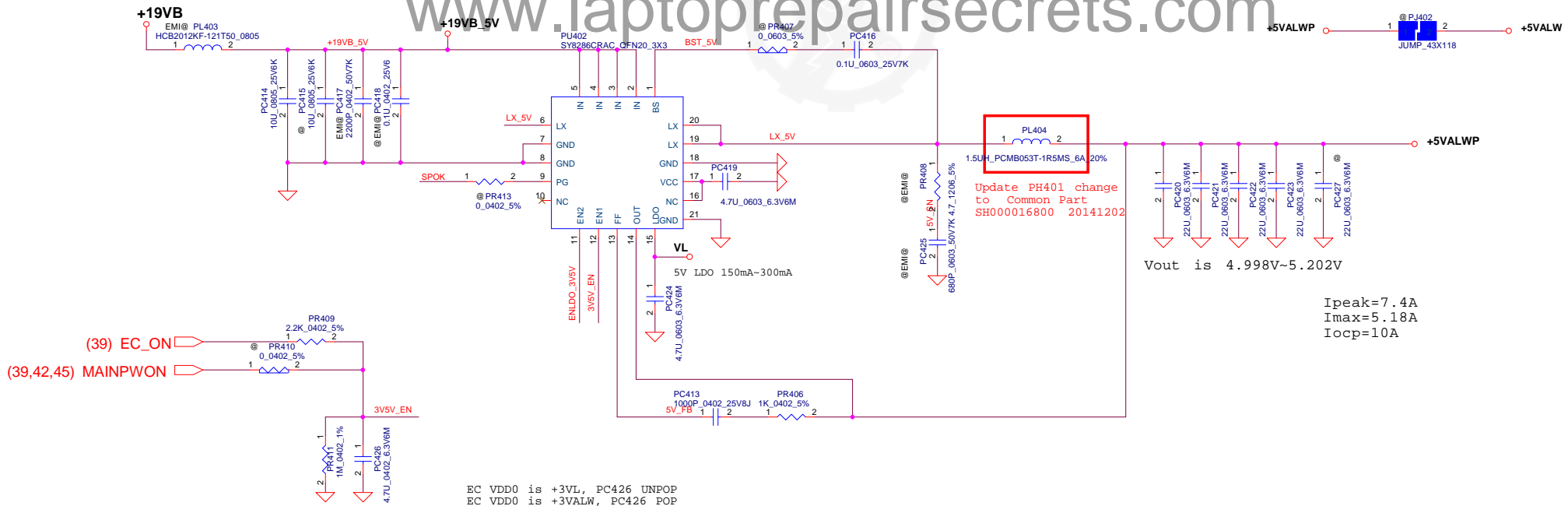
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	BQ24780
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custord	A4WAD M/B LA-C871P
				Date:	Monday, July 13, 2015
				Sheet	46 of 61

SY8208B\_V2.mdd  
SY8208C\_V2.mdd

Vinafix.com



Check pull up resistor of  
SPOK at HW side



Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>PWR-3.3VALWP/5VALWP</b>	
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size Document Number <b>A4WAD M/B LA-C871P</b>	Rev 1.0
				Date: Monday, July 13, 2015	Sheet 47 of 61

RT8207M_V1.mdd	For Single layer
RT8207M_V2.mdd	For Dual layer

Vinatix.com



Switching Frequency: 285kHz  
Ipeak=10A  
Iocp~13A  
OVP: 110%~120%  
VFB=0.75V, Vout=1.3545V  
MOSFET footprint: SIS412DN

Note: S3 - sleep ; S5 - power off

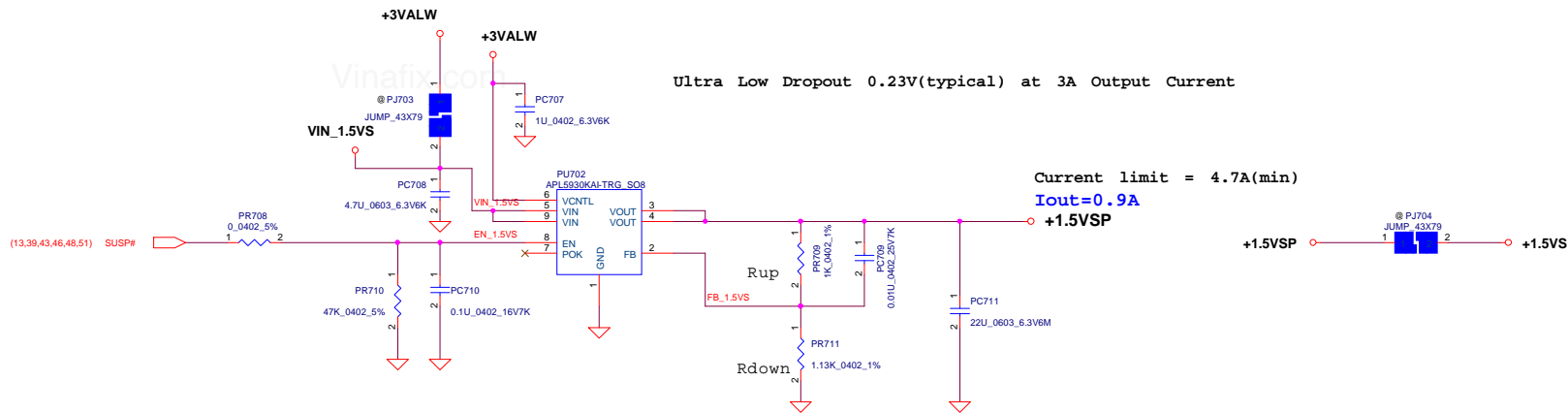
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	RT8207P
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number
				Custom	A4WAD M/B LA-C871P
Date:				Monday, July 13, 2015	Sheet 48 of 61

SYX196D\_V3.mdd



```
Function Field :
VCCEDPIO : IC-35.21 , others - 35.22
VCCEDRAM : IC-35.25 , others - 35.26
```

Security Classification		Compal Secret Data		Compal Electronics, Inc.					
Issued Date		2014/12/31	Deciphered Date		2016/12/31	Title			
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						VCCP			
						Size	Document Number		Rev
						A4AWD M/B LA-C871P			1.0
Date: Monday, July 13, 2015						Sheet 49 of 61			



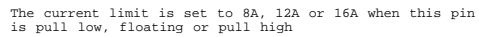
www.laptoprepairsecrets.com

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				SY8032	
Size	Document Number	A4WAD M/B LA-C871P		Rev	1.0
Date:	Monday, July 13, 2015	Sheet	50	of	61



SYX196D\_V3.mdd

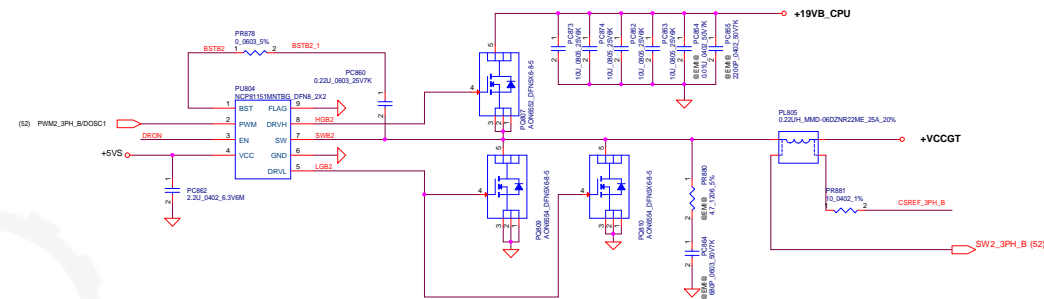
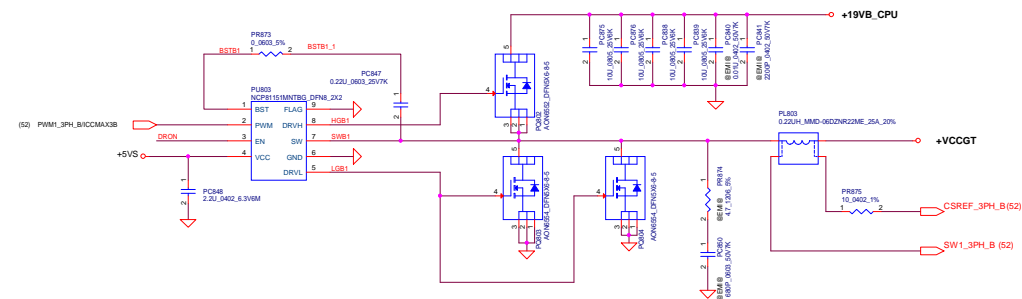
EN pin don't floating  
If have pull down resistor at HW side, pls delete PR2



Pin 7 BYP is for CS.  
Common NB can delete +3VALW and PC15

Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b>		
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title <b>TPS62134</b>		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size C	Document Number	Rev 1.0
				A4WAD M/B LA-C871P		
Date: Monday, July 13, 2015				Sheet	51	of 61



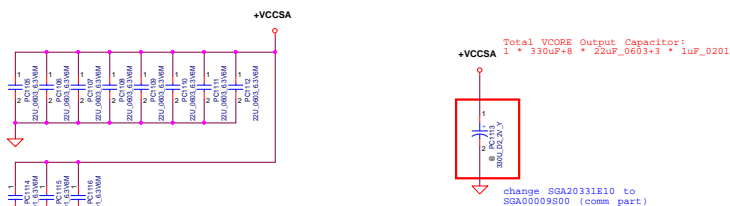
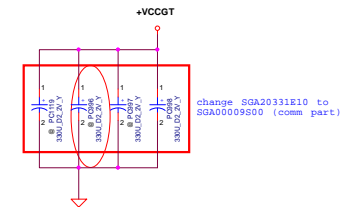
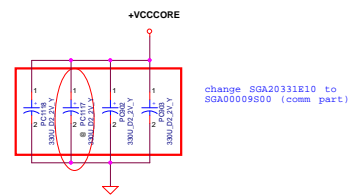
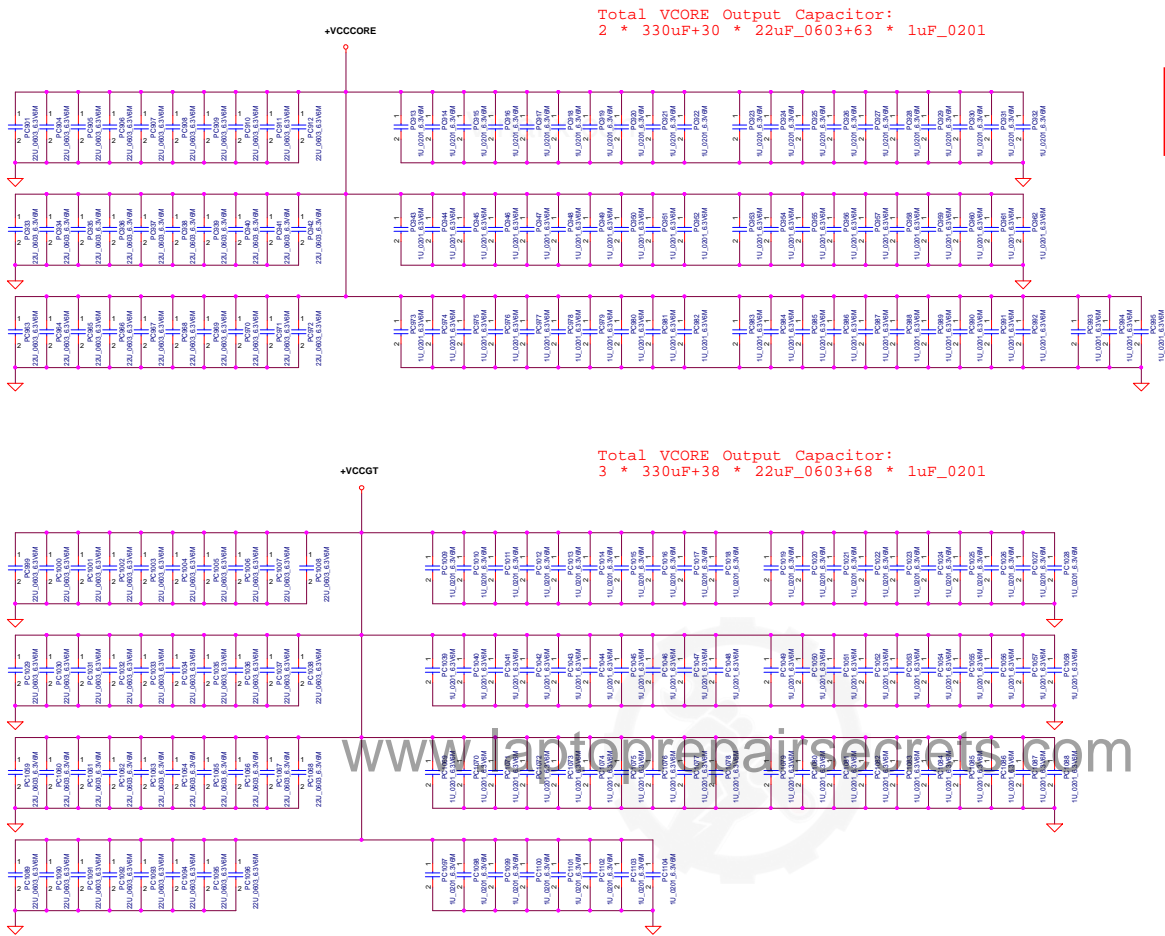


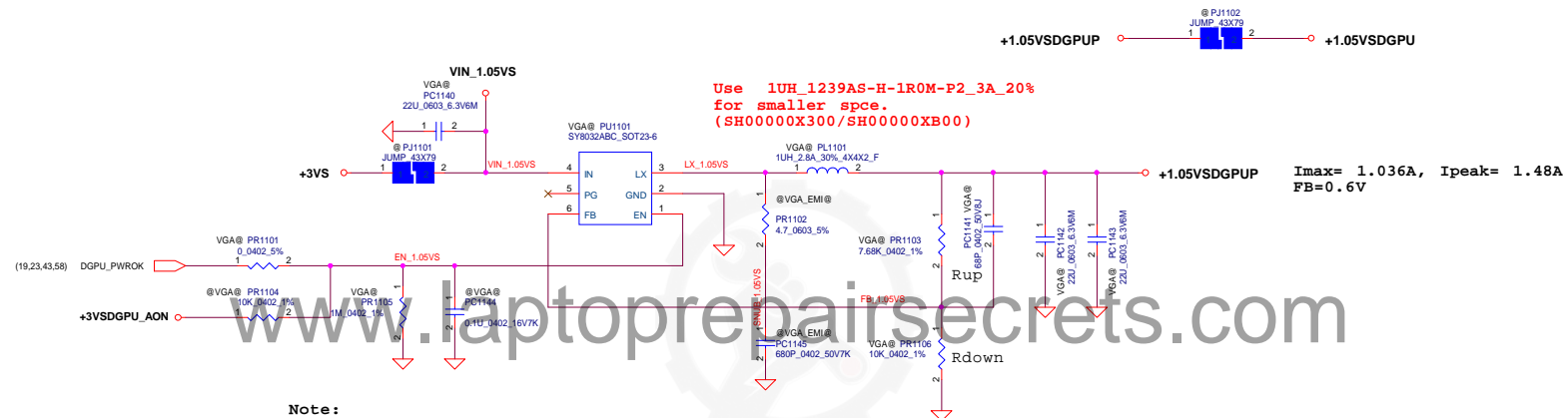
www.laptoprepairsecrets.com

+VCCGT		
TDC 49A		
Peak Current 55A		
OCF current 61A		
Load line mV/A		
FSW=400KHz		
DCR 0.98mohm	+-5%	
	TYP	MAX
L/S Rds(on)	: 6.7mohm	8.5mohm
L/S Rds(on)	: 3mohm	3.7mohm

Security Classification	Compal Secret Data			Title	<b>Compal Electronics, Inc.</b>	
Issued Date	2014/12/31	Deciphered Date	2016/12/31			
THIS SECRET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL INFORMATION. THIS DRAWING IS NOT TO BE REPRODUCED, COPIED, OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC. EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. WITHIN THIS SHEET NO INFORMATION OR CONTENT MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc. Number	Rev	
				104	1.0	
				Drawn	Date	
				AMWAD M/B LA-CH7P		
				Check	Date	
				Monday, July 13, 2015	Sheet 52 of 61	







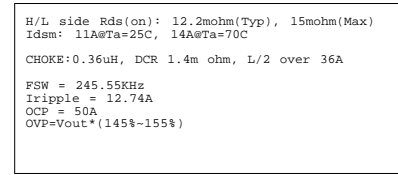
Security Classification		Compal Secret Data		<b><i>Compal Electronics, Inc.</i></b>	
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	<b><i>SY8032</i></b>
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D OR DISCLOSED EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size C	Document Number <b>A4WAD M/B LA-C871P</b>
				Date: Monday, July 13, 2015	Sheet 56 of 61





Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> <b>1.5VSDGPUP</b>	
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Rev
				Document Number	1.0
				A4WAD M/B LA-C871P	
Date:	Monday, July 13, 2015	Sheet	57 of 61		

EN High Threshold = 1.6V



Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2014/12/31	Deciphered Date	2016/12/31	Title	<b>NVIDIA VGA_CORE</b>	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Customer	<b>A4WAD M/B LA-C871P</b>	1.0
				Date:	Monday, July 13, 2015	Sheet 58 of 61

Page 1 of 1  
for PWR

Security Classification	Compal Secret Data			<b>Compal Electronics, Inc.</b>		
Issued Date	2014/11/10	Deciphered Date	2016/12/31	Title <b>P1R</b>		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISIONAL DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Customer	<b>A4WAD M/B LA-C817P</b>	1.0
Date: Monday, July 13, 2015				Sheet	59	of 61

Item	Page	Title	Date	Solution Description		Phase	Rev.
1	6	CMC	3/17	Change XDP to CMC	Change JXDP1 CIS symbol to CMC CIS Symbol(JPCMC1) Rerouting RPC1, RPC2, RPC3, RC56 Del CC1,CC2,CC70,JXDP1,RC12,RC14, RC16,RC18,RC48,RC49,RC50,RC51, RC53,RC54,RC55,RC7,RC9,RPH10 Add JPCMC1,RC59	DVT	0.2
2	9,18,19	CPU,PCH	3/17	change XDP to CMC CONN, reserved test point	Add T3820,T3821,T3822,T3823	DVT	0.2
3	7	CPU	3/17	549401_549401_SKL_H_S_Plat_SMI_WP_Rev0_93	UC1.AU5 UC1.AR8 <DDR_ALERT#> Not used at DDR3L. Tied to GND.	DVT	0.2
4	17	PCH	3/17	Reserved path for TP_INT	Add RH148 0R @	DVT	0.2
5	17	SPI	3/17	546765_546765_2015WW09_Skylake_MOW_Rev_1_0	Change RH28 to @	DVT	0.2
6	31	HDMI	3/17	Reduce unuse part	Del R4962,R4963,R4975	DVT	0.2
7	34	LAN	3/17	Reserved path for +3V_LAN	Add R4984 @ 0_0805_5%	DVT	0.2
8	36	WLAN (M.2)	3/17	follow A4WAS (Requie from Acer) Separate M.2 pin32 and 46 for Intel WLAN 3165	Change "E51RXD_P80CLK_R" to JNGFF1.46	DVT	0.2
9	39	Board ID	3/17	Board ID change to DVT	Change R4903 from 0_0402_5% to 12K_0402_5%	DVT	0.2
10	40	LED	3/17	Follow A4WAD LED Light adjust report	change R1 to 750_0402_1% change R2 to 820_0402_1% change R3 to 180_0402_1% change R6 to 150_0402_1%	DVT	0.2
11	42	BI SW	3/17	Reserved for memory door on D-Cover, place BOT Side	Add SW5 @	DVT	0.2
12	9	PCH	3/20	follow PCH EDS Rev1.5 USB2_ID,USB_VBUSSENSE PD	Add RH149,RH150 1k_0402_5% to GND	DVT	0.2
13	39	EC	3/20	Reserved TPT PU RES	Del R4908,R4910	DVT	0.2
14	39	LID	3/30	EC doesn't internal PU	Change R618 to stuf f	DVT	0.2
15	20	G Sensor	4/1	Reserved	Reserved RH151 PD 100K @ to "G_INT#"	DVT	0.2
16	19	X'TAL	4/8	Change Common part	Change YH1 to S CRYSTAL 32.768KHZ CM7V-T1A9.0PF20PPM	DVT	0.2
17	19	X'TAL	4/8	Follow X'TAL test report	Change CH13 to 10p , CH14 to 8.2p	DVT	0.2
18	19	X'TAL	4/8	Follow X'TAL test report	Change CH11,CH12 to 15p	DVT	0.2
19	18	SMBUS	4/13	Follow INTEL PDG	Change RPH8,RPH9 to 2.2K_0804_8P4R_5%	DVT	0.2
20	41	PC BEEP	4/13	Colay PC_BEEP to EC	Change R2138 to stuf f	DVT	0.2
21	23	NV SMBus	4/13A	Follow INTEL PDG,already conf ir m with NV D A	Change R2000,R2001 to 4.7K_0402_1%	DVT	0.2
22	21	PCH	5/18	Recommend to follow intel PDG decoupling requirement.	add CH54 1u_0402 for UH1.W15 "+3VALW_DSW" change UH1.V28 & AC17 connected to "+1.0VALW_MPHY"	PVT	0.3

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/11/10	Deciphered Date	2016/12/31	Title	PIR-HW1	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	A4WAD M/B LA-C871P	1.0
				Date:	Monday, July 13, 2015	Sheet 60 of 61

Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
23	38	USB charger	5/18	EC control USB charger ic SELCDP	Add NET "USB_SELCDP" for EC control	PVT	0.3
24	16	PCH	5/18	546765_2015WW10_Skylake_MOW_Rev_1_0	change RH150 to 0R, let "USB2_ID" connect to GND change RH149 to 0R, let "USB2_VBUSSENSE" connect to GND	PVT	0.3
25	38	EMC request	5/19	EMC request	Add C4918 33PF_0402 for EMC@	PVT	0.3
26	31,32	HPD	5/19	INTEL request	Change R4985 to STUFF Change R2530 to STUFF	PVT	0.3
27	39	brard ID	5/19	Board ID change to PVT	change R4903 to 15K	PVT	0.3
28	39	brard ID	7/9	Board ID change to PreMP	change R4093 to 20K	Pre-MP	1.0

www.laptoprepairsecrets.com

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/11/10	Deciphered Date	2016/12/31	Title	PIR-HW2	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Size	Document Number	Rev
				Custom	A4WAD M/B LA-C871P	1.0
Date: Monday, July 13, 2015				Sheet	61	of 61